UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STRYKER CORPORATION,

Petitioner

v.

KARL STORZ ENDOSCOPY-AMERICA, INC.,

Patent Owner

Patent No. 7,471,310

Issue Date: December 30, 2008

Title: INTELLIGENT CAMERA HEAD

IPR Number 2015-00673

PETITION FOR *INTER PARTES* REVIEW

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EXHIBITS

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Exhibit 1102: File History Of U.S. Patent No. 7,471,310

Exhibit 1103: U.S. Patent No. 5,701,581 ("Eto")

Exhibit 1104: U.S. Patent No. 6,476,852 ("Okada")

Exhibit 1105: U.S. Patent No. 6,659,940 ("Adler")

Exhibit 1106: Texas Instruments Interface Circuits for TIA/EIA-644 LVDS Design Notes, Nov. 1998 ("TI-LVDS")

Exhibit 1107: U.S. Patent No. 6,608,647 ("King")

Exhibit 1108: U.S. Patent No. 6,278,492 ("Nakamura")

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Exhibit 1110: Service of Complaint in *Karl Storz Endoscopy-America, Inc. v. Stryker Corporation and Stryker Communications, Inc.*, Case No. 14-00876 (N.D. Cal.)

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Stryker Corporation ("Stryker" or "Petitioner") respectfully petitions for *inter partes* review ("IPR") of claims 1-16, 19-22, 25, and 26 of U.S. Patent No. 7,471,310 ("the '310 patent"), which issued on December 30, 2008, and is assigned to Karl Storz Endoscopy-America, Inc. ("KSEA" or "Patent Owner").

I. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Stryker Corporation is the real party-in-interest. Stryker Communications, Inc., a wholly owned subsidiary of Stryker Corporation, is also an interested party.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

KSEA asserted the '310 patent against Stryker in the following patent infringement litigation: *Karl Storz Endoscopy-America, Inc. v. Stryker Corp. and Stryker Comm., Inc.*, Case No. 14-00876 (N.D. Cal.), filed February 26, 2014 ("the litigation"). KSEA served the complaint on Stryker no earlier than March 4, 2014. (Ex. 1110.) No patent applications are pending which claim priority to the '310 patent's application. Stryker has, however, filed a second IPR petition on the same day (IPR2015-00672), asserting invalidity of claims 1-16, 19-22, 25, and 26 of the '310 patent. Stryker has also filed two IPR petitions on U.S. Pat. No. 7,821,530 (which claims priority to the '310 patent"), which are IPR2015-00674 and -00675. Stryker is also concurrently filing petitions for *inter partes* review of the other three patents that KSEA asserted against Stryker in the litigation. (*See* IPR Nos.

2015-00764, 2015-00677, 2015-00678, 2015-00679.)

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel. Pursuant to 37 C.F.R. § 42.8(b)(4), a Power of Attorney accompanies this Petition. Lead Counsel: Robert A. Surrette (Reg. No. 52,262), bsurrette@mcandrews-ip.com. Back-up Counsel: Merle S. Elliott (Reg. No. 52,857), melliott@mcandrews-ip.com; and Christopher Scharff (Reg. No. 53,556), cscharff@mcandrews-ip.com. Post and Delivery: McAndrews, Held & Malloy, 500 West Madison St., 34th Floor, Chicago, IL 60662. Telephone: 312-775-8000. Facsimile: 312-775-8100.

D. Service Information Under 37 C.F.R. § 42.8(b)(4)

Please address all correspondence to the lead counsel at the address provided in Section I.C of this Petition. Petitioner also consents to electronic service by email at: StrykerKSIPR@mcandrews-ip.com.

II. PAYMENT OF FEES – 37 C.F.R. § 41.103

The required fee has been paid online. Please charge any fee deficiencies or credit any overpayments to Deposit Account No. 13-0017.

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R § 42.104

A. Grounds For Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the ‘310 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the ‘310 patent.

B. Identification Of Challenge Under 37 C.F.R. § 42.104(b) And Relief Requested

Petitioner requests *inter partes* review of claims 1-16, 19-22, 25, and 26 of the '310 patent on the grounds set forth below and requests that these claims be found unpatentable. An explanation of how claims 1-16, 19-22, 25, and 26 are unpatentable under specified statutory grounds is provided below, including an identification of where each element is found in the prior art and the relevance of each reference. Additional explanation and support for each ground of rejection is set forth in the Declaration of Dr. John R. Grindon, D. Sc. (Ex. 1109), which is submitted in accordance with 37 C.F.R. § 1.68. *Inter partes* review of claims 1-16, 19-22, 25, 26 is requested in view of the following references:[1]

- U.S. Patent No. 5,701,581 ("Eto") issued December 23, 1997, which is §102(b) prior art (Ex. 1103);
- U.S. Patent No. 6,476,852 ("Okada") filed June 28, 1999, which is §102(e) prior art (Ex. 1104);
- U.S. Patent No. 6,659,940 ("Adler") filed April 5, 2001, which is

[1] The earliest claimed priority date for the '310 patent is December 28, 2001. Without agreeing that the patent claims are entitled to that priority date, for purposes of this IPR any dispute over the priority date does not matter, as each of the asserted references are prior art regardless.

§102(e) prior art (Ex. 1105);

- Texas Instruments Interface Circuits for TIA/EIA-644 LVDS Design Notes, Nov. 1998 ("TI-LVDS") (Ex. 1106), which is §102(b) prior art (Ex. 1106);
- U.S. Patent No. 6,608,647 ("King") filed May 29, 1998, which is §102(e) prior art (Ex. 1107); and
- U.S. Patent No. 4,996,975 ("Nakamura") issued March 5, 1991, which is §102(b) prior art (Ex. 1108).

Ground	Proposed Statutory Rejections for the '310 Patent
1	Claims 1-3, 6, 9-12, 15, 16, 21, and 22 rendered obvious under 35 U.S.C. §103(a) by Eto and Okada
2	Claims 4-5, 7-8, 13-14, 19-20, 25, 26 rendered obvious under 35 U.S.C. §103(a) by Eto, Okada, and Adler
3	Claims 4-5, 7-8, 13-14, 19-20, 25, 26 rendered obvious under 35 U.S.C. §103(a) by Eto, Okada, and TI-LVDS
4	Claims 1-3, 6, 9-12, 15, 16, 21, 22 rendered obvious under 35 U.S.C. §103(a) by Eto, Okada, and King
5	Claims 1, 2, 9-12, 15, 16, 21, 22 rendered obvious under 35 U.S.C. §103(a) by Nakamura and Okada
6	Claims 3-8, 13-14, 19-20, 25-26 rendered obvious under 35 U.S.C.

	§103(a) by Nakamura, Okada, and Adler
7	Claims 3-8, 13-14, 19-20, 25-26 rendered obvious under 35 U.S.C. §103(a) by Nakamura, Okada, and TI-LVDS

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

A claim subject to *inter partes* review is given its "broadest reasonable construction in light of the specification of the patent in which it appears," which may be a broader construction than applied by courts during claim construction.[2] *See* 37 C.F.R. § 42.100(b); *see also Corning Optical Comm. RF, LLC v. PPC Broadband, Inc.*, IPR2013-00340, Paper 79 (P.T.A.B. Nov. 21, 2014); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Further, "[c]onsistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning, as understood by a person of ordinary skill in the art, in the context of the entire patent disclosure." *AOL Inc. v. COHO Licensing, LLC*, IPR2014-00771, Paper 10 (P.T.A.B. Nov. 20, 2014).

Petitioner proposes the following claim constructions:

In independent claims 1, 9, 15, and 21, the claim preamble – **"*[a] video***

[2] Because of the different claim construction standard in litigation, Petitioner reserves all of its rights with regard to constructions during litigation.

***imaging system*"** – does not serve as a claim limitation. A preamble is not limiting when the claim body describes a complete invention such that deletion of the preamble does not affect the structure or steps of the claimed invention. *See, e.g.*, *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1347 (Fed. Cir. 2012) ("[A]s a general rule preamble language is not treated as limiting."); *Marrin v. Griffin*, 599 F.3d 1290, 1294 (Fed. Cir. 2010) ("Preamble language that merely states the purpose or intended use of an invention is generally not treated as limiting the scope of the claim.") Because "[a] video imaging system" describes only the intended use, it is not limiting. (*See* Ex. 1109, Grindon Decl. at ¶ 28.)

In independent claims 1, 9, 15, and 21, a "***camera head***" is "a device that generates an uninterrupted sequence of data that represents moving visual images." (*See* Ex. 1109, Grindon Decl. at ¶ 29.) The remainder of each independent claim recites that the camera head must provide a "stream of digital video data" and the camera control unit processes a "continuous stream of digital video data." (*See, e.g.*, Ex. 1101 at claim 1.) Therefore, it must be a device that generates an uninterrupted (i.e., continuous) sequence of data (i.e., stream of data) representing moving visual images (i.e., video). (*See* Ex. 1109, Grindon Decl. at ¶ 29.)

Moreover, the ***"camera head"*** in claim 1 is <u>not</u> limited to an endoscopic video camera, at least in part because dependent claim 21 is narrower in requiring an endoscope. (*See* Exhibit 1101 at 11:1 (claim 21 adds the limitation of "a

camera head, connected to said cable and an endoscope").) If a "camera head" in claim 1 was limited to an endoscopic video camera, then the quoted language from claim 21 would be redundant. *See Ariosa Diagnostics v. Stanford University*, IPR2013-00308, Paper 40 (P.T.A.B. Nov. 19, 2014) (holding that independent claim necessarily did not include added limitation of dependent claim); *Starhome GmbH v. AT&T Mobility LLC*, 743 F.3d 849, 857-858 (Fed. Cir. 2014) ("The doctrine of claim differentiation is based on the common sense notion that different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope."). The "broadest reasonable construction" of camera head is also obviously not an endoscopic video camera, as that would be a much narrower construction, especially in light of no claim other than claim 21 using the word "endoscope." And during prosecution, the Examiner repeatedly rejected pending claims as anticipated and obvious in view of numerous prior art references that were not directed to endoscopes, and the applicant never argued that those rejections were improper because the references lacked disclosure of an endoscopic video camera. (*See* Ex. 1102, File History of '310 patent at 241-242, 255, 267-268, 294, 313-314.) (*See also* Grindon Decl. at ¶¶ 30-39.)

The remaining terms should receive their broadest reasonable construction.

IV. BACKGROUND OF THE '310 PATENT

The '310 patent generally relates to a video imaging system with

interchangeable camera heads. (*See* Ex. 1109, Grindon Decl. at ¶¶ 17-22; Ex. 1101, '310 patent at Abstract.) The focus of the '310 is the ability for a single camera control unit to control multiple different types of camera heads. (*See id.*)

The '310 patent was filed on December 28, 2001. (*See* Ex. 1101, '310 patent at 1.) During prosecution, the Examiner rejected the pending claims six different times in view of numerous prior art references. (*See* Ex. 1102, File History of '310 patent at 75-92, 126-147, 176-196, 224-246, 277-298, 330-341.) Each time, the applicants amended the claims. (*See id.* at 105-113, 154-161, 201-208, 251-257, 351-356.) In the eventual statements of reasons for allowance, the Examiner stated that the only limitations giving rise to patentable subject matter were "[(1)] the processor in the camera head [(2)] having access to the memory in the camera head that contains camera head information." (*See id.* at 339-340.) The applicants did not respond to the Examiner's statement of reasons for allowance, but rather acquiesced in the Examiner's statement and amended the rejected base claims to incorporate these two limitations. (*See id.* at 351-356.) As shown throughout this petition and supporting declaration, however, even these two limitations were well-known in the art before the data of the alleged invention.

V. ELEMENT-BY-ELEMENT ANALYSIS OF HOW CHALLENGED CLAIMS ARE UNPATENTABLE (37 C.F.R. §§42.104)

There is a reasonable likelihood that claims 1-16, 19-22, 25, and 26 are unpatentable because they are rendered obvious in view of the prior art.

A. Ground 1: Claims 1-3, 6, 9-12, 15, 16, 21, and 22 are Obvious Under 35 U.S.C. § 103(a) by Eto and Okada (Processor and Memory Reference)

Claims 1-3, 6, 9-12, 15, 16, 21, and 22 are obvious under 35 U.S.C. § 103(a) in view of Eto in combination with Okada.

As discussed in detail below, Eto discloses a general video imaging system that comprises a camera control unit, a cable, and a camera head. The camera head of Eto includes an imager, a timing generator, a converter, a serializer, a digital serial driver, a digital serial receiver, a multiplexer, and a processor. The camera control unit of Eto includes a digital serial receiver and a digital serial driver that is controlled based at least in part upon the timing signal.

Okada, meanwhile, also discloses a video imaging system having a camera head and a camera control unit. The camera head of Okada, however, includes a processor and memory device containing information about the camera head. The memory device of Okada is accessible to the processor. Further, Okada expressly discloses that the video imaging system can be used in an endoscope.

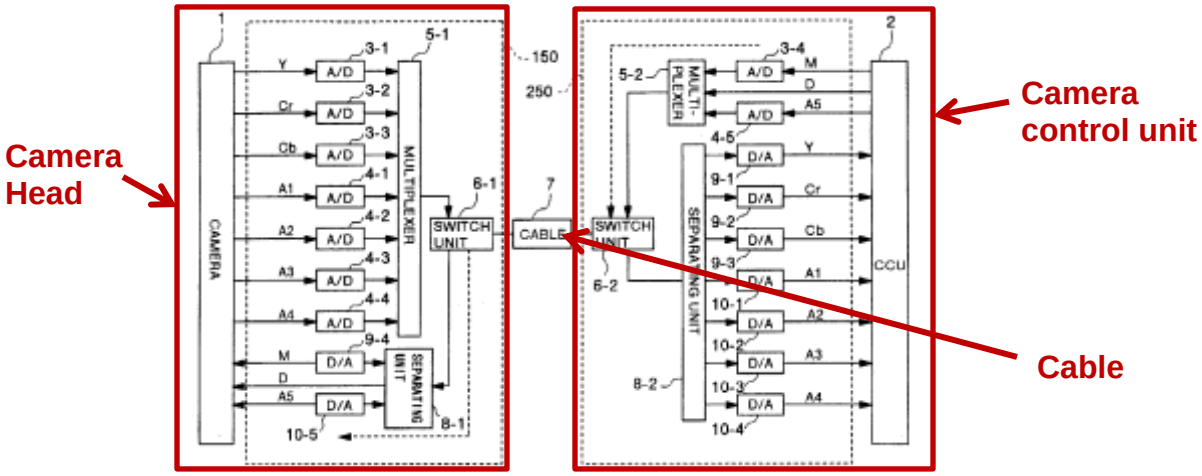
For the reasons discussed below, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention of the ‘310 patent to include a processor and memory in the camera head of Eto, as taught by Okada. Such a combination satisfies all of the elements of claims 1-3, 6, 9-12, 15, and 16. Further, it would have been obvious to also use the imaging system of Eto in an

endoscope, as taught by Okada. Such a combination satisfies the additional limitations of claims 21 and 22.

(i) Independent claims 1, 9, and 15

Independent claims 1, 9, and 15 contain most of the same claim elements, each of which is found in the combination of Eto and Okada.

First, to the extent the preamble is limiting, Eto discloses a "*video imaging system*." Eto's video imaging system comprises a camera head, a cable, and a camera control unit, as shown below in Fig. 1:



(Ex. 1103, Eto at Fig. 1 (annotated); *see also* Eto at 13:47-49, 1:8-14 ("[t]he present invention relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU', i.e., Camera Control Unit) are coupled with each other. . . .").) (*See also* Ex. 1109, Grindon Decl. at ¶ 55.)

Second, Eto discloses a "*camera control unit processing a continuous*

stream of digital video data" as recited by claims 1, 9, and 15. Eto discloses that it "relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU,' i.e., Camera Control Unit) are coupled with each other by employing a single transmission path through which a video signal, an audio signal, and a control signal are multiplexed and transmitted in a bidirectional manner." (Ex. 1103, Eto at 1:8-14 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶¶ 56-57.) "On both of the camera side and the CCU side, the signals are processed by way of the digitalizing process, the time-divisional multiplexing process, the time-axis compressing process." (Ex. 1103, Eto at 4:54-57.) A person of ordinary skill in the art would recognize that Eto's "transmitting/receiving apparatus 250" and "CCU 2" (hereinafter, "Eto's camera control unit") is "a camera control unit processing a continuous stream of digital video data." (*See* Ex. 1109, Grindon Decl. at ¶ 57.)

Third, Eto discloses a "*cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera unit*," as required by claims 1, 9, and 15. Eto discloses a "cable" in, for example, Figure 1. (*See* Ex. 1103, Eto at Fig. 1.) Eto also discloses that "digital signals are transmitted via the cable in the digital code form." (Ex. 1103, Eto at 3:43-48.) (*See also* Ex. 1109, Grindon Decl. at ¶ 58.)

Fourth, Eto discloses a "*camera head, connected to said cable, for providing*

the stream of digital video data," as recited by claims 1, 9, and 15. Eto explains that "a video (picture) signal obtained from a television camera 1 is three sorts of video signals" which are "analog video signals [that] are A/D-converted . . . into digital video signals." (Ex. 1103, Eto at 7:7-18.) The digital videos signals are then transmitted to the CCU. (*Id.* at 7:66-81.) A person of ordinary skill in the art would recognize that Eto's "transmitting/receiving apparatus 150" and "camera 1" (hereinafter, "Eto's camera head") is a "camera head, connected to said cable, for providing the stream of digital video data." (*See also* Ex. 1109, Grindon Decl. at ¶ 59.)

Fifth, Eto discloses an "*imager, for generating an analog stream of video data*" as recited in claims 1 and 15. Figure 1 of Eto shows the imager (i.e., the Y, Cr, and Cb analog video components of the camera). (*See* Ex. 1103, Eto at Fig. 1.) Further, Eto states that this imager is for generating an analog stream of video data. It states that "a video (picture) signal obtained from a television camera 1 is three sorts of video signals, i.e., a luminance signal 'Y' and two sorts color difference signals 'Cr' and 'Cb' instead of the respective video signals R, G, B. . . . These three sorts of analog video signals are A/D-converted . . . ." (Ex. 1103, Eto at 7:7-19; Ex. 1109, Grindon Decl. at ¶ 60.)

Eto also discloses an "*imager, for generating the stream of digital video data*," as recited in claim 9. Eto explains that "a video (picture) signal obtained

from a television camera 1 is three sorts of video signals" which are "analog video signals [that] are A/D-converted by A/D converters 3-1, 3-2, 3-3 of a transmitting/receiving apparatus 150 into digital video signals." (Ex. 1103, Eto at 7:7-18.) Therefore, the image sensor generates the Y, Cr, and Cb analog video components of a video signal that is then digitized by A/D converters 3-1, 3-2, 3-3. This combination of an imager and analog-to-digital converter is also how the '310 patent achieves "an imager, for generating the digital stream of video data." As the Examiner pointed out during prosecution, "the only type of image signal that the specification discloses the imager generating is an analog image signal." (*See* Ex. 1102, File History of '310 patent at 130.) The applicants agreed with the Examiner and amended what is now claim 21 to recite "an imager, including an analog to digital converter for generating a digital image signal." (*Id.* at 160.) However, a later amendment to what is now claim 9 apparently inadvertently reverted back to "an imager, for generating the stream of digital video data." (*Id.* at 253.) Thus, to the extent that "an imager, for generating the stream of digital video data" as recited in claim 9 is supported at all by the specification of the 310 patent, it is necessarily the combination of an imager and analog-to-digital converter, which is what Eto discloses. (*See* Ex. 1109, Grindon Decl. at ¶ 61.)

Sixth, Okada discloses *"a timing generator, generating a timing signal particular to said camera head, the timing signal actuating said imager and sent to*

said camera control unit," as recited in claims 1 and 9 (but not in 15). Okada describes that "on the scope side" is a "timing generator 16." (Ex. 1104, Okada at 4:4-15, Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35 ("In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525).") Okada moreover provides a timing generator particular to the camera head that actuates the imager. (*See, for example*, Ex. 1104, Okada at Fig. 1.) The four components 16, 17, 18, and 19 of the camera head comprise a timing generator that is configurable for either PAL or NTSC cameras by camera head CPU 20 using configuration information stored in camera head ROM 21. (*See* Ex. 1109, Grindon Decl. at ¶ 62.) The timing generator 16 is in the camera head, and the imaging memory 24A is in the camera control unit. In order for the picture data to be written into the imaging memory "in the timing of the synchronization signal formed in the timing generator 16," the synchronization signal must be sent to the camera control unit which contains the imaging memory. (*See id; see also* Ex. 1104, Okada at 5:48-56.) Therefore, as disclosed by Okada, the timing generator

16 in the camera head (scope side) must send a timing synchronization signal to the CCU (processor side), used to write the transferred picture data into memory 24 on the camera control unit, or CCU. (*See id.*) Because Okada discloses that the timing generator is configurable for either PAL or NTSC, the timing generator generates a timing signal particular to said camera head. The timing signal of Okada thus actuates the imager and is sent to the camera control unit. (*See* Ex. 1109, Grindon Decl. at ¶ 62.)

It would have been obvious in view of Okada to provide a timing generator in Eto particular to the camera head to actuate the imager. (*See id.* at ¶ 63) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) Namely, including the timing signal generator in the camera head, and sending that timing signal to the camera control unit would have been obvious because such a timing signal would allow for the interchangeability of camera heads and synchronization of the camera head and camera control unit. (*See id.*) Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*)

Seventh, Eto discloses a "*converter, for converting the analog stream of*

video data into the stream of digital video data" as recited by claims 1 and 15 (claim 9 does not include this limitation). Eto states that on the camera head, the "analog video signals are A/D-converted by A/D converters 3-1, 3-2, 3-3 of a transmitting/receiving apparatus 150 into digital video signals." (Ex. 1103, Eto at 7:7-19, Fig. 1.) (*See also* Ex. 1109, Grindon Decl. at ¶ 64.)

Eighth, Eto discloses "*a serializer, for serializing the stream of digital video data for transmission over said cable*," as recited in claims 1 and 15 (but not in 9). Eto describes that "[t]he camera 101 outputs the digitalized video signal" which is "converted into serial data by parallel-to-serial converting circuit 104." (Eto at 15:6-15 (emphasis added).) (*See also*, Ex. 1109, Grindon Decl. at ¶ 65.)

Ninth, Eto discloses "*at least one digital serial driver*," as recited in claims 1 and 9 (but not in 5). As discussed, Eto discloses transmitting a serial signal over cable 110 to the CCU 118 side. The structure in Eto that drives the digital serial signal is the "data output gate 120." (Ex. 1103 at 16:44-48; *see also* Ex. 1109, Grindon Decl. at ¶ 66.) Alternatively, transmitting a serial digital signal over a cable necessarily and inherently requires a driver to drive the signal. (*See id.*)

Tenth and eleventh, the claimed "*processor*" on the camera head and "*memory device, accessible by said processor, containing camera head information*," as recited by claims 1, 9, and 15 are found Okada. Okada discloses a "first CPU" on the "scope side" (i.e., camera head). (Ex. 1104, Okada at 4:4-15.)

The CPU "controls the total" of the timing circuits and switching and constitutes "a processor." (*Id.*) (*See also* Ex. 1109, Grindon Decl. at ¶¶ 67-69.) Okada discloses a "ROM" memory on the "scope side." (Ex. 1104, Okada at Fig. 1.) Okada discloses that "to the first CPU 20 [on the camera head] a ROM 21 storing setting data . . . is connected." (*Id.* at 4:16-28.) And Okada discloses that "the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit . . ." (*Id.* at 4:58-5:3.) The "setting data" is camera head information. (*See* Ex. 1109, Grindon Decl. at ¶ 68.)

It would have been obvious in view of Okada to provide a processor and a memory device in Eto's camera head to enable the use of different camera heads. (*See* Ex. 1109, Grindon Decl. at ¶ 69.) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) Namely, including a processor with access to a memory in the camera head would be advantageous because such a processor and memory would allow for local processing and use of the information in the memory. (*See id.*) At the time of the alleged invention, the advantages of interchangeable camera heads were well-known. (*See id.*) It would have been obvious to employ the processors and memory including information about the camera head in a video imaging system because providing for different camera heads would be advantageous to allow

multiple camera heads with different capabilities, replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*)

Twelfth, Eto discloses "*said camera control unit having at least one digital serial receiver*," as recited in claims 1 and 9 (but not in 15). This limitation is satisfied by the "data fetching gate 121" of Eto, which receives the digital serial data signal. (Ex. 1103, Eto at 16:36-43, Ex. 1109, Grindon Decl. at ¶ 70.) Alternatively, this limitation is again inherent in Eto by virtue of its disclosure of transmitting digital serial information over a cable from a camera to a control unit. One of ordinary skill in the art would have known that transmitting a serial digital signal over a cable necessarily and inherently requires a digital serial receiver to receive the digital serial signal that is transmitted. (*See id.*)

Thirteenth, the combination of Eto and Okada satisfies the limitation that the camera control unit is "*controlled based at least in part upon said timing signal particular to said camera head*," as recited in claims 1 and 9 (but not in 15). Okada discloses a "timing generator" and discloses that on the control unit side, "picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B. . . Then, each of these signals of R, G, and B is outputted to a monitor . . ." (Ex.

1104 at 5:21-35 (emphasis added).) Thus, the camera control unit is controlled based at least in part by the timing signal. (Ex. 1109, Grindon Decl. at ¶ 71.)

Including the timing signal generator in the camera head and sending that timing signal to at least partially control the camera control unit would have been obvious because such a timing signal would allow for interchangeable camera heads and synchronization of the camera head and camera control unit. (*See id.* at ¶ 72.) Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*) Interchangeability of camera heads would be useful to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*)

Fourteenth, the combination of Eto and Okada would have rendered obvious the final additional limitation of independent claim 9 (which is not found in claims 1 or 15) that "*a plurality of camera heads, each with differing timing signals, are attachable to and controlled by said camera control unit*." Okada provides for the interchangeability of two different types of cameras having differing timing

signals, i.e., NTSC and PAL. (Ex. 1104, Okada at 6:10-19.) Further, for the reasons discussed above, adding a memory and processor in a camera head would have enabled interchangeable camera heads. (*See* Ex. 1109, Grindon Decl. at ¶¶ 73-74.) Interchangeable camera heads would allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Providing interchangeable camera heads to the imaging system of Eto would have involved merely the use of a known technique to improve a similar system in the same way, and/or the predictable use of prior art elements according to their established functions. (*See id.*)

(ii) Claims 2, 11, and 16:

Eto discloses that "*said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals*." Eto states that "The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are multiplexed in the time-divisional multiplexing circuit 102, are compressed with respect to the time axis in time axis compressing circuit 103, and thereafter are converted into serial data by parallel-to-serial converting circuit 104." (Ex. 1103, Eto 581 at 15:6-11.) (*See also* Ex. 1109, Grindon Decl. at ¶ 77.)

(iii) Claims 3, 6

Eto discloses that "*said camera head utilizes at least one digital serial*

receiver," as recited by claim 3, and that "*said camera control unit utilizes at least one digital serial driver*," as recited by claim 6. Eto states that the "signals which have been multiplexed in a time-divisional multiplexing circuit 115 are compressed with respect to the time axis in a time-axis compressing circuit 112, and the compressed signals are converted into serial data by a parallel-to-serial converting circuit 111. The resultant serial data constitutes a transmission signal on the CCU side as shown in FIG. 12, and then this transmission signal is transmitted via a cable 110 to a transmitting/receiving apparatus 123 on the camera 110 side." (Ex. 1103, Eto at 14:50-58.) Thus, a serial digital signal is transmitted from the CCU, over the cable, and to the camera head. (*See* Ex. 1109, Grindon Decl. at ¶ 78.) Transmitting a serial digital signal over a cable from the CCU to the camera head would necessarily require a receiver on the camera head to receive the signal, and a driver on the CCU to drive the signal. (*See id.*)

(iv) Claim 10

Eto discloses that "*said camera head produces analog image data, said camera head further comprising a converter, for converting an analog image signal to a digital image signal*," as required by claim 10 (this element is also discussed above with respect to independent claim 1). Eto 581 discloses that "a video (picture) signal obtained from a television camera 1 is three sorts of video signals, i.e., a luminance signal 'Y' and two sorts color difference signals 'Cr' and

'Cb' instead of the respective video signals R, G, B. . . . These three sorts of analog video signals are A/D-converted by A/D converters 3-1, 3-2, 3-3 of a transmitting/receiving apparatus 150 into digital video signals." (Ex. 1103, Eto at 7:7-19 and Fig. 1.) (*See also* Ex. 1109, Grindon Decl. at ¶¶ 79-80.)

(v) Claim 12

Eto discloses that "*said camera head further comprises a serializer, for serializing the image signal*," as required by claim 12 (this element is also discussed above with respect to claim 1). Eto discloses a "parallel/serial converting circuit 104" on the camera head, which converts the digitalized video signal, audio signal, and control signal into "serial data." (*See* Ex. 1103, Eto at Fig. 11 and 15:6-15.) (*See also* Ex. 1109, Grindon Decl. at ¶ 81.)

(vi) Claims 21, 22

Eto in combination with Okada also discloses the use of the claimed video imaging system in an endoscope, as recited in independent claim 21 and dependent claim 22. Independent claim 21 for the most part recites the same limitations variously found in claims 1, 9, and 15, except for a "*camera head connected . . . to an endoscope*." And claim 22 only adds the same limitation found in claims 2, 11, and 16 of a "*multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals*." For the same reasons discussed above and in the below claim chart, the combination of Eto and Okada discloses each of

the limitations that are identically found in claims 21 and 22 versus claims 1, 2, 9, 11, 15, or 16. (*See above* at §V.A.i. and claim chart.)

Claim 21 does contains one limitation that differs slightly from claims 1, 9, and 15. Claim 21 recites "*an imager, including an analog to digital converter for generating the stream of digital video data*," rather than (as recited in claim 1) an "*imager, for generating an analog stream of video data*" and a "*converter, for converting the analog stream of video data into the stream of digital video data*." (*See* Ex. 1101, claims 1 and 21.) Eto, however, discloses this feature. As the Examiner stated during prosecution of the '310 patent (and the applicant agreed), "the only type of image signal that the ['310 patent] specification discloses the imager generating is an analog image signal." (*See* Ex. 1102, File History of '310 patent at 130.) Therefore, this element is met with disclosure of "an imager" and "an analog to digital converter," the result of which is "for generating the stream of digital video data." Eto discloses an imager and analog to digital converter for generating the stream of digital video data. (*See above* at §V.A.1; Ex. 1103, Eto at Fig. 1 (disclosing imager and A/D converter).)

Unlike claims 1, 9, and 15, claim 21 includes "*a camera head, connected to said cable and an endoscope.*" (*See below* at claim chart; Ex. 1109, Grindon Decl. at ¶¶ 82-92.) Okada, however, specifically discloses that it "relates to an imaging device for an endoscope." (Ex. 1104, Okada at 1:12-16 and Fig. 1.) Okada

discloses that the camera is connected on the "scope side." (*Id.* at Fig. 1.) It was well-known in the art that an endoscope could be connected to a camera head. Thus, the combination of Eto, which expressly discloses a camera head, and Okada, which expressly discloses an endoscope, renders obvious this limitation of claim 21. (*See* Ex. 1009, Grindon Decl. at ¶ 92.)

It would have been obvious in view of Eto and Okada to use the combined video imaging system in an endoscope. (*See also* Ex. 1109, Grindon Decl. at ¶¶ 93-96.) Such a combination would have involved only combining systems according to known methods to yield predictable results and/or the use of a known technique to improve a similar system in the same way. (*See id.*) Namely, the combination would have involved only using an improved camera system in a specific new application, i.e., an endoscope, in the identical way. (*See id.*) Eto and Okada are very similar in components, capabilities, and function. (*See id.* at ¶ 95.) There is nothing unique about a camera system having a separate camera head/camera control unit system in an endoscope versus in another device. (*See id.*) The same basic components disclosed in Eto are also used with endoscopes. (*See id*.) A person of ordinary skill in the art would have looked to video imaging technology in multiple industries when designing any video imaging system. (*See id.*) The advantages of doing so have been recognized in the prior art. (*See id.*)

(vii) Lack of Secondary Considerations

There are also no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any secondary considerations having a nexus to the claimed invention. (*Id.* at ¶ 97.)

(viii) Claim Charts

The below claim charts shows how the combination of Eto and Okada discloses each element of claims 1-3, 6, 9-12, 15, 16, 21, and 22 of the '310 patent.

'310 Patent Claims 1, 9, 15, 21	**Eto in Combination With Okada**
(1, 9, 15, 21) A video imaging system comprising:	Ex. 1103, Eto '581 at 1:8-14, 7:7-9, 13:47-49, Figs. 1, 11. Ex. 1104, Okada 852 at 3:58-61, 1:12-16, Fig. 1.
(1, 9, 15, 21) a camera control unit processing a continuous stream of digital video data;	Ex. 1103, Eto '581 at 1:8-14, 4:44-53, 4:54-57, 7:7-18, 7:66-8:4. Ex. 1104, Okada '852 at 4:34-40.
(1, 9, 15, 21) a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	Ex. 1103, Eto '581 at 3:43-48, Figs. 1, 11.
(1, 9, 15) a camera head, connected to said cable, for providing the stream of digital video data, said camera head including;	Ex. 1103, Eto '581 at 7:7-19, Figs. 1, 11. Ex. 1104, Okada '852 at 4:4-15.
(21) a camera head, connected to said cable and an endoscope, for providing the stream of digital video data, said camera head including;	Ex. 1104, Okada '852 at 4:4-15, Fig. 1.
(1, 15) an imager, for generating an	Ex. 1103, Eto '581 at 7:7-19, Figs. 1,

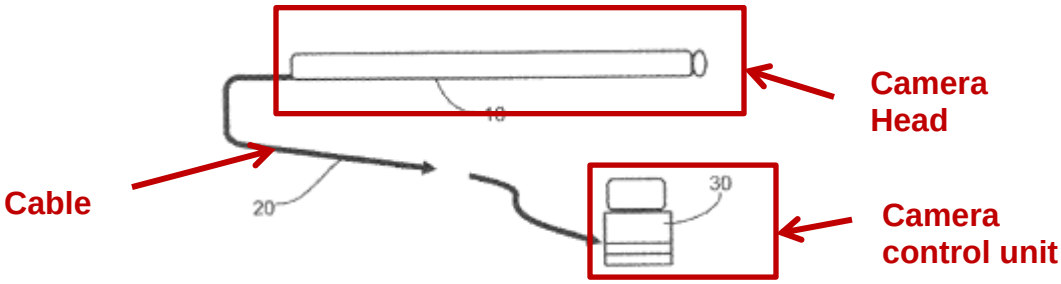
analog stream of video data; *(9) an imager, for generating the stream of digital video data;* *(21) an imager, including an analog to digital converter for generating the stream of digital video data*	11. Ex. 1104, Okada '851 at 4:4-15, Fig. 1.
(1, 9, 15) a timing generator, generating a timing signal particular to said camera head, the timing signal actuating said imager and sent to said camera control unit	Ex. 1104, Okada '852 at 4:4-15, Fig. 1, 5:4-20, 5:21-35, 5:48-56.
(1, 15) a converter, for converting the analog stream of video data into the stream of digital video data	Ex. 1103, Eto '581 at 7:7-19, Figs. 1 and 11. Ex. 1104, Okada '852 at 4:29-33.
(1, 15, 21) a serializer, for serializing the stream of digital video data for transmission over said cable	Ex. 1103, Eto '581 at 15:6-15.
(1, 9) at least one digital serial driver;	Ex. 1103, Eto '581 at 15:6-15.
(1, 9, 15, 21) a processor; and	Ex. 1104, Okada '852 at 4:4-15, Fig. 1.
(1, 9, 15, 21) a memory device, accessible by said processor, containing camera head information	Ex. 1104, Okada 852 at 4:16-28, 4:4-15, Okada at 4:16-28, 4:58-5:3.
(1, 9) said camera control unit having at least one digital serial receiver	Ex. 1103, Eto '581 at 15:6-15, Fig. 11.
(1, 9) and is controlled based at least in part upon said timing signal particular to said camera head.	Ex. 1103, Eto 581 at 15:6-22. Ex. 1104, Okada '852 at 4:58-5:3,

	5:21-35, Fig. 1, 4:58-5:20.
(9 only) wherein a plurality of camera heads, each with differing timing signals, are attachable to and controlled by said camera control unit.	Ex. 1104, Okada '852 at 4:58-5:3, 5:21-35, Fig. 1, 4:58-5:20, 6:10-19.
'310 Patent, Claims 2, 11, 16, 22	**Eto in Combination With Okada**
(2, 11, 16, 22) The video imaging system according to claim 1[or claim 9, 15, or 22] wherein said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals.	Ex. 1103, Eto 581 at 15:6-11, 14:50-58.
'310 Patent, Claim 3	**Eto in Combination With Okada**
3. The video imaging system according to claim 1 wherein said camera head utilizes at least one digital serial receiver.	Ex. 1103, Eto '581 at 15:6-15.
'310 Patent, Claim 6	**Eto in Combination With Okada**
6. The video imaging system according to claim 1 wherein said camera control unit utilizes at least one digital serial driver.	Ex. 1103, Eto '581 at 15:6-15.
'310 Patent, Claim 10	**Eto in Combination With Okada**
10. The video imaging system according to claim 9 wherein said camera head produces analog image data, said camera head further comprising a converter, for converting an analog image signal to a digital image signal.	Ex. 1103, Eto at 7:7-19, Figs. 1 and 11. Ex. 1104, Okada '852 at 4:29-33.
'310 Patent, Claim 12	**Eto in Combination With Okada**
12. The video imaging system according to claim 9 wherein said camera head further comprises a serializer, for serializing the image signal.	Ex. 1103, Eto '581 at 15:6-15.

B. Ground 2: Claims 4-5, 7-8, 13-14, 19-20, 25, 26 Are Obvious in View of Eto, Okada (Processor and Memory Reference) and Adler (LVDS Reference)

Claims 4-5, 7-8, 13-14, 19-20, and 25-26 recite digital serial drivers and digital serial receivers in the camera head and camera control unit that utilize Low-Voltage Differential Signals (LVDS). (*See* Ex. 1101, '310 patent at claims 4, 5, 7, 8, 13, 14, 19, 20, 25, 26.) As discussed above, Eto in combination with Okada would have rendered obvious all of the features of independent claims 1, 9, 15, and 21. It would have been further obvious in view of Adler to use LVDS in such a video system, which would have satisfied all of the limitations of claims 4-5, 7-8, 13-14, 19-20, and 25-26.

Specifically, Adler teaches a video imaging system for an endoscope, comprising a camera head, camera control unit, and cable, as shown below:



(Ex. 1105, Adler at Fig. 1 (annotated), 9:24-38; Ex. 1109, Grindon Decl. at ¶ 100.) Just like Eto and Okada, the camera control unit of Adler processes a continuous stream of digital video data from the camera head, through a cable. (*See, e.g.*, Ex. 1105, Adler at 9:24-33 ("The configuration comprises a miniature endoscopic . . . attached by a wire connection 20 to a processing device 30. . ."), 9:39-47, 5:21-23

("Preferably, the dedicated image processor is a motion video processor . . . .").)

Adler, however, states that it specifically uses LVDS data transmission. Adler states that "[t]he electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Ex. 1105, Adler at 10:7-19.) (*See also* Ex. 1109, Grindon Decl. at ¶ 101.) One of ordinary skill in the art would have recognized that LVDS is a communications protocol that is particularly appropriate for video applications because it has a high bit rate. (*See* Ex. 1109, Grindon Decl. at ¶ 102.)

It would have been obvious to employ the high bit rate LVDS communication protocol in the video imaging system of Eto in combination with Okada because the combination would have involved merely the combination of known elements to achieve a predictable result. (*See* Ex. 1109, Grindon Decl. at ¶ 103.) One of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system. (*See id.*) Thus, one of ordinary skill in the art would have easily incorporated Adler's LVDS components in Eto's camera head and control unit because Eto already discloses that digital serial data is transmitted using drivers and receivers. (*See id.*) The result would be predictable; that is, the resulting video imaging system would merely use a

different serial communication protocol to transmit information between the camera head and camera control unit. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. LVDS is particularly appropriate for video applications due to high data rates, lower power, and adaptability to lower voltages. (*See id.* at ¶ 104.) It would have been obvious to employ the high bit rate of LVDS in the video imaging system of Eto/Okada because a higher bit rate is more advantageous in video applications because it can transfer data more quickly. (*See id.*) LVDS would have improved the combination in the same way as Adler. (*See id*.)

Additionally, the combination would have been obvious because Adler contains a teaching, suggestion, and motivation to use LVDS in an endoscopic system. The combination of Eto and Okada would result in an endoscopic video imaging system that discloses every limitation of claims 1-3, 6, 9-12, 15, 16, 21, and 22. Adler further teaches the use of LVDS in an endoscopic video imaging system. One of ordinary skill in the art would have read that disclosure in Adler as a motivation to use LVDS in the Eto/Okada endoscopic video imaging system. (*See* Ex. 1109, Grindon Decl. at ¶ 105.)

There are also no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 106.)

C. Ground 3: Claims 4-5, 7-8, 13-14, 19-20, 25, 26 Are Obvious in View of Eto, Okada (Processor and Memory Reference) and TI-LVDS (LVDS Reference II)

As discussed above in Ground 2, it would have been obvious at the time of the alleged invention of the '310 patent to substitute LVDS as the digital serial communication protocol in the combination of Eto and Okada. In Ground 2, Petitioner relied on Adler for disclosure of LVDS in a camera system very similar to those of Eto and Okada. Adler, however, is prior art under 35 U.S.C. §102(e). Should the Board determine that Patent Owner KSEA is able to swear behind Adler as prior art, there are numerous other §102(b) prior art references disclosing LVDS as a serial communication protocol, including the TI-LVDS reference. Accordingly, Ground 3 is non-redundant to Ground 2, because Ground 3 relies on §102(b) prior art for LVDS instead of §102(e) prior art.

The LVDS standard, formally known as TIA/EIA-644 Low-Voltage Differential Signaling, was created by Texas Instruments as "a signaling method used for high-speed, low-power transmission of binary data over copper." (Ex. 1106, TI-LVDS at 6.) Exhibit 1106 (the TI-LVDS reference) is cited on the face of the '310 patent as prior art non-patent literature. (*See* Ex. 1101, '310 patent at

1.) In fact, the '310 patent references digital serial drivers and digital serial receivers manufactured by Texas Instruments that implement the LVDS standard. (*See, e.g.*, Ex. 1101, '310 patent at 6:49-55, 6:64-7:1, 7:64-8:3, 8:13-17, 8:51-57.) Figure 1 of TI-LVDS shows "a typical connection with LVDS drivers and receivers." (Ex. 1106, TI-LVDS at 6-7.) Thus, the use of LVDS for transmitting digital data was well-known prior to the alleged '310 patent invention. (*See* Ex. 1109, Grindon Decl. at ¶¶ 109-110.)

For reasons similar to those discussed above with respect to Eto, Okada, and Adler, it would have been obvious to utilize the LVDS communication protocol in TI-LVDS in the combination of Eto and Okada. One of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system. (*See id.* at ¶¶ 111-116.) One of ordinary skill in the art would have recognized the benefits of LVDS as disclosed in TI-LVDS, such as very high bit rates (655 Mbit/s), low power consumption, and adaptability to low voltage levels, all of which are particularly suitable for small imaging devices, such as endoscopes. (*See id.*) The combination would involve the known method of simply replacing Eto/Okada's digital serial drivers and receivers with comparable LVDS modules. (*See id.)* The result would be predictable; that is, the resulting video imaging system would merely use a different serial communication protocol

to transmit information between the camera head and camera control unit. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. As explained above, LVDS would have improved the Eto/Okada system by providing for a higher bit rate that would allow the transmission of high resolution endoscopic video images. (*See id*.) LVDS would have improved the combination in the same way as the TI-LVDS reference. (*See id.*)

There are also no secondary considerations of which Petitioner is aware that would tend to show that the combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 118.)

D. Ground 4: Claims 1-3, 6, 9-12, 15, 16, 21, and 22 Are Obvious Under 35 U.S.C. §103(a) in View of Eto, Okada (Processor and Memory Reference) and King (Timing Signal Reference)

As discussed above, Eto in combination with Okada would have rendered obvious all of the features of independent claims 1, 9, 15, and 21. This includes the requirement of *"a timing generator, generating a timing signal particular to said camera head, the timing signal actuating said imager and sent to said camera control unit,"* as found in independent claims 1 and 9 (independent claims 15 and 21 do not include this limitation). It also includes the requirement of "*a plurality*

of camera heads, each with differing timing signals, are attachable to and controlled by said camera control unit," as found in independent claim 9. Alternatively, even if these elements were not disclosed in the combination of Eto and Okada, it would have been obvious to include these features in view of King.

King discloses a video imaging system including a camera head (34) and a camera control unit (36). (Ex. 1107, King at Fig. 1.) The camera head includes a CCD image sensor and a CCD timing generator (42). (Ex. 1107, King at Fig. 2 (annotated) and 5:51-58; Ex. 1109, Grindon Decl. at ¶ 121.) The timing generator (42) generates a timing signal particular to the camera head that actuates the imager, and this timing signal is sent to the camera control unit. (*See* King at 6:20-36 (describing "CCD Timing Generator 42"); 6:4-12 ("Along with the image signal, the CHU 34 returns a clocking signal, PCLCK, that indicates the timing of the video signal and a data valid signal, DATA VALID_L, identifying that portion of the video signal containing valid image data."), 5:9-20 ("The final step, the readout cycle, is used to move or output the charges to the Camera Head Unit, which combines them with timing information to form an image signal for application to the Camera Control Unit (CCU)."") (emphasis added). (*See also* Ex. 1109, Grindon Decl. at ¶¶ 121-123.)

King states that use of a timing generator in each camera head allows the use of different, interchangeable camera heads. (*See* Ex. 1107, King at 6:41-55

("Since a single Camera Control Unit (CCU) 36 preferably supports configurations with multiple Camera Head Units (CHUs), a set of shutter (C0 Shutter_L . . . Cn Shutter_L) and readout (C0 Readout_L . . . Cn Readout_L) controls are derived for each potentially installed CHU. Similarly the Acquire Timing Generator 44 accepts the pixel clock (C0 PCLK . . . Cn PCLK), data validation signals (C0 DataValid_L . . . Cn DataValid_L), and video wave forms (C0 Video . . . Cn Video) from each installed CHU.") (emphasis added).)

It would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '310 patent to combine Eto, Okada, and King. (*See* Ex. 1109, Grindon Decl. at ¶¶ 124-127.) Including the timing signal generator in the camera head, and sending that timing signal to the camera control unit as claimed in the '310 patent, would have been obvious because such a timing signal would allow for the interchangeability of camera heads and synchronization of the camera head and camera control unit. (*See id*.) Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*) One of ordinary skill in the art would have looked to other video imaging systems to conclude this. (*See id*.) Moreover, the advantages of interchangeable camera heads were well-known—interchangeable camera heads permits

replacement camera heads in the event of malfunction, or different camera heads for different circumstances. (*See id*.)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '310 patent to add timing signal generator of King to Eto and Okada because the combination involved combining known elements according to known methods to yield predictable results (i.e., adding a timing generator on the camera head would allow different camera heads to synchronize with the camera control unit, would have predictably enabled interchangeable camera heads). (*See* Ex. 1109, Grindon Decl. at ¶ 125.)

Alternatively, the combination would have been obvious because the combination results from the use of a known technique to improve a similar system in the same way, the application of a known technique to a known system that is ready for improvement, to yield predictable results, or a known work in a field of endeavor prompting predictable variations of it, based on design incentives or other market forces (i.e., it would have been obvious to add a timing generator to the camera head of Eto and Okada to improve the system by enabling interchangeable camera heads). (*See id.* at ¶ 126.)

Additionally, the combination would have been obvious because it would have involved merely the predictable use of prior art elements according to their established functions. (*See* Ex. 1109, Grindon Decl. at ¶ 127.) One of ordinary

skill in the art would have looked to other video imaging systems to conclude that a timing signal generator in the camera head would be an obvious way to implement interchangeable camera heads and synchronize the camera control unit and the camera head. (*See id*.) At the time of the alleged invention of the '310 patent, the advantages of interchangeable camera heads were well-known. (*See id*.) Enabling the interchangeability of camera heads would have also been useful, for example, where the camera head is mounted on tooling or robots that require different camera heads for different uses or for a smaller size camera head if it were to be required to fit into tight spaces. (*See id*.) Interchangeability among camera heads would also have been useful for different types of industrial inspections and for different types of dangerous environments, where the camera head must be separated from the camera control unit or shaped differently depending on the circumstances. (*See id*.)

There are also no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 128.)

E. Ground 5: Claims 1, 2, 9-12, 15, 16, 21, 22 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura and Okada (Processor and Memory Reference)

Claims 1, 2, 9-12, 15, 16, 21, and 22 are also obvious under 35 U.S.C. § 103(a) in view of Nakamura in combination with Okada. Similar to Eto,

Nakamura discloses a video imaging system that comprises a camera control unit, a cable, and a camera head. Okada, meanwhile, again also discloses a video imaging system including a camera head and a camera control unit. The camera head of Okada includes a processor and memory containing information about the camera head. Further, Okada expressly discloses that the video imaging system can be used in an endoscope.

For the reasons below, it would have been obvious to include a processor and memory in the camera head of Nakamura, as taught by Okada. Such a combination would satisfy all of the elements of claims 1-2, 9-12, 15, and 16. Further, it would have been obvious to also use the imaging system of Nakamura in an endoscope, as taught by Okada. Such a combination would satisfy the additional limitations of claims 21 and 22.

(i) Independent claims 1, 9, and 15

All of the elements of independent claims 1, 9, and 15 (which again largely overlap) are found in the combination of Nakamura and Okada.

First, to the extent the preamble is limiting, Nakamura discloses a "*video imaging system*." Nakamura's video imaging system comprises a camera, a cable, and a camera control unit, as shown below in Fig. 2:

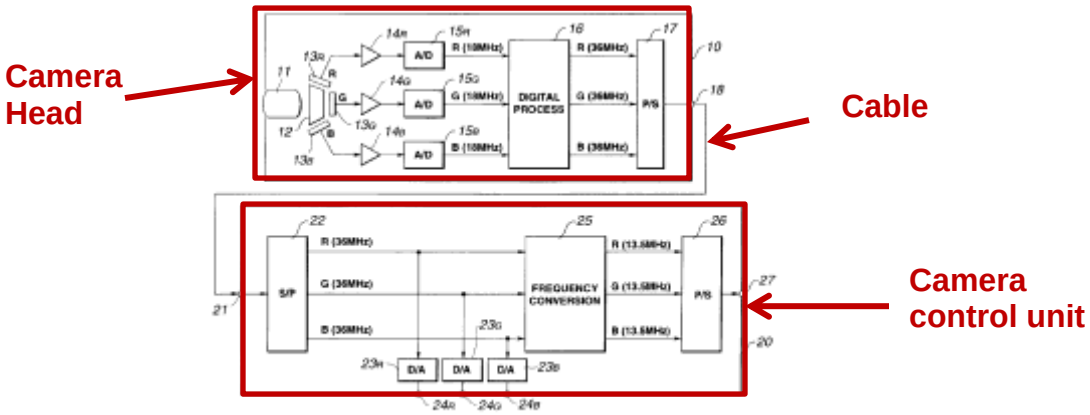


FIG.2

(Ex. 1108, Nakamura at Fig. 2 (annotated); *see also* Nakamura at 1:8-10 ("a method and apparatus for transmitting digital video signals obtained on imaging by a CCD imaging device."), 4:25-26.) (See also Ex. 1109, Grindon Decl. at ¶ 133.)

Second, Nakamura discloses a "*camera control unit processing a continuous stream of digital video data*" as recited by claims 1, 9, and 15. (*See* Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20. The serial digital video signals of R, G and B, supplied to the camera control unit 20, are converted . . . into R, G and B component digital video signals.") (emphasis added) (*See also* Ex. 1109, Grindon Decl. at ¶ 134.)

Third, Nakamura discloses a "*cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera unit*," as required by claims 1, 9, and 15. (*See* Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20.") (emphasis added).

(*See also* Ex. 1109, Grindon Decl. at ¶ 135.)

Fourth, Nakamura discloses a "*camera head, connected to said cable, for providing the stream of digital video data*," as recited by claims 1, 9, and 15. Figure 2 of Nakamura (shown above) illustrates the "camera" connected to the cable. (*See* Ex. 1108, Nakamura at Fig. 2; *id.* at 4:27-46 ("Referring to FIG. 2, the light from an object, incident on a lens system 11 of a camera head 10, is sent to a color-separation prism 12. . . . In the camera head shown in FIG. 2, the CCDs 13R, 13G and 13B are arranged so that the CCDs 13R and 13B for R and B are horizontally offset by one-half the pixel pitch with respect to the CCD 13G for G.") (emphasis added); *id.* at 5:23-30 ("Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 18, compatibility in format is maintained between the camera head 10 and the camera control unit.") (*See also* Ex. 1109, Grindon Decl. at ¶ 136.)

Fifth, Nakamura discloses an "*imager, for generating an analog stream of video data*" as recited in claims 1 and 15. Nakamura states that "[t]he lens system 11 includes . . . a lens for imaging the light from the object on a CCD . . . ." (Ex. 1108, Nakamura at 4:27-39.) (*See also id.* at 4:40-54 ("These R, G and B light beams are converted by the associated CCDs 13R, 13G and 13B into imaging signals associated with R, G and B, respectively. . . The imaging signals for R, G and B from the CCDs 13R, 13G and 13b . . . are subsequently converted into

digital imaging signals by analog/digital (A/D) conversion circuits . . .").) In other words, the image signals generated by the camera head are analog signals. (*See also* Ex. 1109, Grindon Decl. at ¶ 137.) Additionally, Nakamura discloses "*an imager, for generating the stream of digital video data*," as recited by claim 9. Again, this limitation applies to a separate imager and analog-to-digital converter, because that is all the '310 patent discloses. (*See above*.) Nakamura discloses that "R, G and B light beams are converted by the associated CCDs 13R, 13G and 13B into imaging signals associated with R, G and B, respectively. . . .The imaging signals for R, G and B from the CCDs 13R, 13G and 13b . . . are subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits . . . ." (Ex. 1108, Nakamura at 4:40-54.) Therefore, CCDs 13R, 13G, and 13B generate an analog stream of video data, which is then digitized by A/D conversion circuits, the result of which is "an imager, for generating the digital stream of video data." (*See* Ex. 1109, Grindon Decl. at ¶ 138.)

Sixth, Nakamura discloses "*a timing generator, generating a timing signal particular to said camera head, the timing signal actuating said imager and sent to said camera control unit*," as required by claims 1 and 9 (claim 15 does not include this limitation). Nakamura states that "[t]he A/D conversion circuits 15R, 15G and 15B digitally convert the analog imaging signals, using the clocks of the same frequency as that of the sampling clocks in the CCDs 13R, 13G and 13B. . . ."

(Ex. 1108, Nakamura 492 at 4:54-64, Fig. 2, 5:48-61.) The processes that occur in the camera head, such as analog-to-digital conversion, digital signal processing, and frequency conversion, all require timing signals generated by a timing generator. (*See* Ex. 1109, Grindon Decl. at 139-141.) A person of ordinary skill in the art would know that the timing for the CCD devices must be derived form a timing source in common with the clock signals that drive these processes to maintain synchronization. (*See id.*) Thus, the timing signal used to actuate the imager is embedded in the serial data signal sent to the CCU. (*See id.*)

Alternatively, this element is disclosed in Okada, which describes "on the scope side" a "timing generator 16." (Ex. 1104, Okada at 4:4-15, Fig. 1, 5:4-20 Okada also states that "if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1." (*Id.* at 5:21-35.) The timing signal of Okada thus actuates the imager and is sent to the camera control unit. (*See also* Ex. 1109, Grindon Decl. at ¶ 142.)

To the extent not already disclosed in Nakamura, it would have been obvious in view of Okada to provide a timing generator particular to the camera head to actuate the imager. (*See id.* at ¶ 143.) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or combining prior art elements according to known methods to yield

predictable results. (*See id.*) Specifically, including the timing signal generator in the camera head, and sending that timing signal to the camera control unit would have been an improvement to allow for the interchangeability of camera heads. (*See id.*) Using the known method of allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit, would predictably allow the two devices to remain synchronized even with a plurality of different camera heads. (*See id.*)

Seventh, Nakamura discloses a "*converter, for converting the analog stream of video data into the stream of digital video data*" as recited by claims 1 and 15 (claim 9 does not include this limitation). Nakamura discloses that "[t]he imaging signals for R, G and B from the CCDs 13R, 13G and 13B are amplified by associated pre-amplifiers 14R, 14G and 14B, respectively, and subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits 15R, 15G and 15B, respectively." (Ex. 1108, Nakamura at 4:50-64 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 144.)

Eighth, Nakamura discloses "*a serializer, for serializing the stream of digital video data for transmission over said cable*," as required by claims 1 and 15 (claim 9 does not require this limitation). Nakamura discloses that "[t]he above-mentioned R, G and B component digital video signals, obtained by the digital processing circuit 16, are converted by a P/S [parallel to serial] conversion circuit

17 into serial composite digital video signals which are outputted along with various other sorts of the information at the output terminal 18." (Ex. 1108, Nakamura at 5:18-23.) These "serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20." (*Id.* at 5:27-29.) (*See* Ex. 1109, Grindon Decl. at ¶ 145.)

Ninth, Nakamura discloses "*at least one digital serial driver,*" as recited by claims 1 and 9 (claim 15 does not recite this limitation). The parallel to serial conversion circuit of Nakamura outputs the serial signal to the output terminal, and from that to the input terminal and serial to parallel conversion circuit of the camera control unit. (Ex. 1108, Nakamura at Fig. 2, 5:18-29.) In other words, the parallel to serial conversion circuit of Nakamura functions as a digital serial driver. (*See* Ex. 1109, Grindon Decl. at ¶ 146.) Moreover, one of ordinary skill in the art would have understood at the time of the alleged invention that transmitting a serial digital cable from an output terminal over a cable must inherently involve a driver to drive the digital serial signal. (*See* Ex. 1109, Grindon Decl. at ¶ 146.)

Tenth and eleventh, the claimed "*processor*" on the camera head and "*memory device, accessible by said processor, containing camera head information,*" as recited by claims 1, 9, and 15, are found in Okada. (*See above* at Section V.A.(i), discussing the disclosure in Okada of the claimed processor and memory device.) It would have been obvious in view of Okada to provide a

processor and memory on the camera head, to enable the use of different camera heads. (*See* Ex. 1109, Grindon Decl. at ¶¶ 147-148.) Doing so would have involved merely the use of a known technique to improve a similar system in the same way, and/or the predictable use of prior art elements according to their established functions. (*See id.*) One of ordinary skill in the art would have concluded that a processor on the camera head would be an obvious way to implement the use of different or interchangeable camera heads. (*See id.*) Including the claimed processor and memory would allow for local processing and use of information regarding each camera head in the memory. (*See id.*) A person of ordinary skill in the art would have known that interchangeable camera heads would allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*)

Twelfth, Nakamura discloses "*said camera control unit having at least one digital serial receiver*," as recited by claims 1 and 9 (claim 15 does not contain this limitation). This limitation is again expressly found in Nakamura by virtue of it disclosing an input terminal and a serial-to-parallel conversion circuit, which receives the digital serial signal sent over the cable from the camera head. (*See* Ex. 1109, Grindon Decl. at ¶ 149.) Moreover, one of ordinary skill in the art would have known that transmitting a serial digital signal over a cable must necessarily and inherently requires a digital serial receiver to receive the digital serial signal

that is transmitted. (*See id*.)

Thirteenth, Nakamura discloses that the camera control unit is "*controlled based at least in part upon said timing signal particular to said camera head*," as recited by claims 1 and 9 (claim 15 does not contain this limitation). Nakamura describes that the timing signal transmitted from the camera head to the control unit sets the limit resolution of the camera control unit (i.e., "controls" the camera control unit). (*See* Ex. 1108, Nakamura at 5:48-61 ("[T]he limit resolution obtained from the 36 MHz rate digital video signals obtained with the digital processing circuit 206 [sic: inadvertently refers to FIG. 1] of the camera head 200 [sic: inadvertently refers to FIG. 1] is ideally approximately 1400. This rate is maintained when the digital video signals are transmitted to the camera control unit 20. . . . That is, since the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks . . .").) (*See also* Ex. 1109, Grindon Decl. at ¶ 150.)

Alternatively, Okada again discloses a "timing generator" and discloses that "picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory . . . . Then, each of these signals of R, G, and B is outputted to a monitor . . ." (Ex. 1104, Okada at 5:21-35.) Thus, the camera control unit is "controlled" at least

partly by the timing signal. (*See* Ex. 1109, Grindon Decl. at ¶ 151.)

Including the timing signal generator in the camera head and sending that timing signal to at least partially control the camera control unit would have been obvious because such a timing signal would allow for the interchangeability of camera heads and synchronization of the camera head and camera control unit. (*See id.* at ¶ 152.) Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*) Again, interchangeable camera heads would have been advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Doing so would have involved a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*)

Fourteenth, the combination of Nakamura and Okada would have rendered obvious the final additional limitation of independent claim 9 (which is not found in claims 1 or 15) of "*a plurality of camera heads, each with differing timing signals, [] attachable to and controlled by said camera control unit*." For the reasons discussed above, adding a memory and processor in a camera head would have enabled interchangeable camera heads, which would have been an

improvement over a single-camera imaging system. (*See supra*.) For example, interchangeable camera heads would be advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Providing interchangeable camera heads to the imaging system of Nakamura would have involved merely the use of a known technique to improve a similar system in the same way, and/or the predictable use of prior art elements according to their established functions. (*See id.*)

(ii) Claims 2, 11, and 16:

Nakamura discloses that "*said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals*." The '310 patent states that "[c]ontrol signals include any signal transmitted from the camera head except image data." (Ex. 1101, '310 patent at 4:1-2.). Nakamura states that "R,G and B component digital video signals . . . are outputted along with various other sorts of the information at an output terminal 18." (Ex. 1108, Nakamura 492 at 5:18-26 (emphasis added).) Because the serial composite video signals "are outputted along with various other sorts of the information," the composite video signals necessarily and inherently must be multiplexed. (*See also* Ex. 1109, Grindon Decl. at ¶ 157.) Moreover, the control signals from the sampling clocks of the CCD are inherently embedded in the composite video signals. (*See id*.)

(iii) Claim 10

Nakamura discloses that "*said camera head produces analog image data, said camera head further comprising a converter, for converting an analog image signal to a digital image signal*," as required by claim 10 (this element is also discussed above with respect to independent claim 1). Nakamura discloses that "[t]he imaging signals for R, G and B from the CCDs 13R, 13G and 13B are amplified by associated pre-amplifiers 14R, 14G and 14B, respectively, and subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits 15R, 15G and 15B, respectively.") (Ex. 1108, Nakamura at 4:50-64 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 158.)

(iv) Claim 12

Nakamura discloses that "*said camera head further comprises a serializer, for serializing the image signal*," as required by claim 12 (this element is also discussed above with respect to claim 1). Nakamura discloses that "[t]he above-mentioned R, G and B component digital video signals, obtained by the digital processing circuit 16, are converted by a P/S [parallel to serial] conversion circuit 17 into serial composite digital video signals which are outputted along with various other sorts of the information at the output terminal 18." (Ex. 1108, Nakamura at 5:18-23.) These "serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera

control unit 20." (*Id.* at 5:27-29.) (*See also* Ex. 1109, Grindon Decl. at ¶ 160.)

(v) Claims 21, 22

Nakamura also discloses the use of the claimed video imaging system in an endoscope, as required by independent claim 21 and dependent claim 22. Independent claim 21 for the most part recites the same limitations variously found in claims 1, 9, and 15, but adds the requirement of "*a camera head, connected to said cable and an endoscope*." And claim 22 only adds the same limitation found in claims 2, 11, and 16 of a "*multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals*."

For the same reasons discussed above and in the below claim chart, the combination of Nakamura and Okada discloses each of the limitations that are identically found in claims 21 and 22 versus claims 1, 2, 9, 11, 15, or 16.[3] (*See above* at §V.E.i. and claim chart.) The combination of Nakamura and Okada also

[3] Claim 21 also slightly differently recites "*an imager, including an analog to digital converter for generating the stream of digital video data*," rather than (as recited in claim 1) an "*imager, for generating an analog stream of video data*" and a "*converter, for converting the analog stream of video data into the stream of digital video data*." (*See* Ex. 1101, claims 1 and 21.) As discussed in the below claim chart, Nakamura discloses this slightly differently-recited limitation of claim 21. (*See below* at claim chart; *see also* Ex. 1109, Grindon Decl. at ¶-.)

would have disclosed connecting the camera head to an endoscope, as required by claims 21 and 22. Okada discloses that it "relates to an imaging device for an endoscope." (Ex. 1104, Okada at 1:12-16 and Fig. 1.) The camera is connected on the "scope side." (*Id.* at Fig. 1.) (*See* Ex. 1109, Grindon Decl. at ¶¶ 161-171.)

It would have been obvious in view of Nakamura and Okada to use the video imaging system in an endoscope. (*See also* Ex. 1109, Grindon Decl. at ¶¶ 172-175.) Due to the very close similarities in components, capabilities, and function, between Nakamura and Okada, it would have been obvious to use the technology of Nakamura in an endoscope as disclosed by Okada. (*See id.*) There is nothing unique about a camera system having a separate camera head/camera control unit system in an endoscope versus in another device. (*See id*.) The same size considerations, need for interchangeability, analog-to-digital requirements, processing requirements, etc. exist in, for example, Nakamura's system, as would exist in an endoscope. (*See id*.) Such a combination would have involved only combining systems according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, the use of a known technique to improve a similar system in the same way, and/or the predictable use of known prior art elements according to their established functions. (*See id*.) A person of ordinary skill in the art would have looked to video imaging technology in multiple industries, not just the field of endoscopes,

when designing any video imaging system. (*See id.*) (*See also*, above at Ground 1 (discussing prior art references describing how general video imaging technology is applicable to endoscopes).)

(vi) Lack of Secondary Considerations

There are no secondary considerations of which Petitioner is aware that would tend to show that the combination of Nakamura and Okada is non-obvious—particularly any secondary considerations having a nexus to the claimed invention. (*See* Ex. 1109, Grindon Decl. at ¶ 176.)

(vii) Claim Charts

The below claim charts shows how Nakamura and Okada disclose each element of claims 1, 2, 9-12, 15, 16, 21, and 22 of the '310 patent.

'310 Patent Claims 1, 9, 15, 21	**Nakamura in Combination With Okada**
(1, 9, 15, 21) A video imaging system comprising:	Ex. 1108, Nakamura '492 at Fig. 2, 1:8-10, 4:25-26. Ex. 1104, Okada 852 at 3:58-61, 1:12-16, Fig. 1.)
(1, 9, 15, 21) a camera control unit processing a continuous stream of digital video data;	Ex. 1108, Nakamura '492 at Fig. 2 and 5:27-33. Ex. 1104, Okada '852 at 4:34-40.
(1, 9, 15, 21) a cable, connected to said camera control unit, for transmitting the stream of digital video data to said camera control unit; and	Ex. 1108, Nakamura '492 at Fig. 2 and 5:27-33.

(1, 9, 15) a camera head, connected to said cable, for providing the stream of digital video data, said camera head including;	Ex. 1108, Nakamura '492 at Fig. 2, 4:27-46, 5:23-30, 5:27-33. Ex. 1104, Okada '852 at 4:4-15.
(21) a camera head, connected to said cable and an endoscope, for providing the stream of digital video data, said camera head including;	Ex. 1104, Okada '852 at 4:4-15.
(1, 15) an imager, for generating an analog stream of video data; *(9) an imager, for generating the stream of digital video data;* *(21) an imager, including an analog to digital converter for generating the stream of digital video data*	Ex. 1108, Nakamura '492 at 4:27-39, 4:40-54. Ex. 1104, Okada '851 at 4:4-15, Fig. 1.
(1, 9, 15) a timing generator, generating a timing signal particular to said camera head, the timing signal actuating said imager and sent to said camera control unit	Ex. 1108, Nakamura 492 at 4:54-64, Fig. 2, 5:48-61, 5:18-30. Ex. 1104, Okada '852 at 4:4-15, Fig. 1, 5:4-20, 5:21-35, 5:48-56.
(1, 15) a converter, for converting the analog stream of video data into the stream of digital video data	Ex. 1108, Nakamura '492 at 4:50-64, Fig. 2. Ex. 1104, Okada '852 at 4:29-33.
(1, 15, 21) a serializer, for serializing the stream of digital video data for transmission over said cable	Ex. 1108, Nakamura '492 at 5:18-23, 5:27-29.
(1, 9) at least one digital serial driver;	Ex. 1108, Nakamura '492 at 5:18-23, 5:27-29.
(1, 9, 15, 21) a processor; and	Ex. 1104, Okada '852 at 4:4-15, Fig.

	1.
(1, 9, 15, 21) a memory device, accessible by said processor, containing camera head information	Ex. 1104, Okada 852 at 4:16-28, Fig. 1, 4:58-5:3, 4:4-15, 4:16-28, 4:58-5:3.
(1, 9) said camera control unit having at least one digital serial receiver	Ex. 1108, Nakamura '492 at 5:27-29.
(1, 9) and is controlled based at least in part upon said timing signal particular to said camera head.	Ex. 1108, Nakamura '492 at 5:48-61. Ex. 1104, Okada '852 at 4:58-5:3, 5:21-35, Fig. 1, 4:58-5:20.
(9 only) wherein a plurality of camera heads, each with differing timing signals, are attachable to and controlled by said camera control unit.	Ex. 1104, Okada '852 at 4:58-5:3, 5:21-35, Fig. 1, 4:58-5:20.
'310 Patent, Claims 2, 11, 16, 22	**Nakamura in Combination With Okada**
(2, 11, 16, 22) The video imaging system according to claim 1[or claim 9, 15, or 22] wherein said camera head further comprises a multiplexer, for generating a multiplexed signal, which includes the digital image signal and control signals.	Ex. 1108, Nakamura 492 at 5:18-26.
'310 Patent, Claim 10	**Nakamura in Combination With Okada**
10. The video imaging system according to claim 9 wherein said camera head produces analog image data, said camera head further comprising a converter, for converting an analog image signal to a digital image signal.	Ex. 1108, Nakamura '492 at 4:27-39, 4:40-54, 4:50-64, Fig. 2. Ex. 1104, Okada '852 at 4:29-33.
'310 Patent, Claim 12	**Nakamura in Combination With Okada**
12. The video imaging system according	Ex. 1108, Nakamura '492 at 5:18-23,

to claim 9 wherein said camera head further comprises a serializer, for serializing the image signal.	5:27-29.

F. Ground 6: Claims 3-8, 13-14, 19-20, 25-26 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura, Okada (Processor and Memory Reference) and Adler (LVDS Reference)

As discussed above in Section V.D., Nakamura in combination with Okada would have rendered obvious all of the features of independent claims 1, 9, 15, and 21. In addition, it would have been further obvious in view of Adler to use LVDS in such a video system. Doing so would have satisfied all of the limitations of claims 4-5, 7-8, 13-14, 19-20, and 25-26. Further, it would have been obvious in view of Adler to provide a digital serial receiver in the camera head and a digital serial driver in the camera control unit (for transmission of data from the camera control unit to the camera, as opposed to just the other way around). Such a combination would have satisfied claims 3 and 6.

Adler teaches a video imaging system for an endoscope, comprising a camera head, camera control unit, and cable. (Ex. 1105, Adler at Fig. 1; *see also id.* at 9:24-38, 9:24-33, 9:39-47, 5:21-2. Adler, however, specifically discloses LVDS data transmission. Adler states that "[t]he electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Ex. 1105, Adler at 10:7-19 (emphasis added).) (*See also* Ex. 1109,

Grindon Decl. at ¶¶ 179-180.) One of ordinary skill in the art would have recognized that LVDS is a communications protocol that is particularly appropriate for video applications because it offers high bit rates. (*See* Ex. 1109, Grindon Decl. at ¶ 183.)

Adler also discloses that "[c]ontrol data from the processing device 30 is preferably received at the endoscope 40 by a receiving device 64, which may typically be an LVDS receiver. Hard wired logic 66 preferably serves as an interface to convert the incoming control data into signals for controlling both the sensor 46 and the light source 50." (Adler at 10:20-29.) In a system that supports bidirectional communication, the camera head necessarily utilizes at least one digital receiver and the camera control unit utilizes at least one digital driver. (*See* Ex. 1109, Grindon Decl. at ¶¶ 181-182.)

It would have been obvious to employ the high bit rate LVDS communication protocol in the video imaging system of Nakamura in combination with Okada, for the same reasons as discussed above with respect to Eto, Okada, and Adler. The combination would have involved merely combining known elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, and/or the application of a known technique to a known system that is ready for improvement, to yield predictable results. (*See* Ex. 1109, Grindon Decl. at ¶¶ 183-

186.) Again, a higher bit rate can transfer video image data more quickly. (*See id*.) Further, it would have been obvious to employ both a digital receiver and transmitter in each of the camera head and camera control unit, in order to provide bidirectional communication. (*See id*.) Bidirectional communication would have provided control of the camera head from the control unit. (*See id*.)

There are no secondary considerations of which Petitioner is aware that would tend to show that the combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 187.)

G. Ground 7: Claims 3-8, 13-14, 19-20, 25-26 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura, Okada (Processor and Memory Reference) and TI-LVDS (LVDS Reference II)

As discussed above in Ground 6, it would have been obvious at the time of the alleged invention of the '310 patent to substitute LVDS as the digital serial communication protocol in the combination of Nakamura and Okada, as well as utilize bi-directional drivers and receivers. In Ground 6, Petitioner relied on Adler for disclosure of LVDS and bi-directional drivers and receivers in a camera system very similar to those of Nakamura and Okada. Adler, however, is again prior art under 35 U.S.C. §102(e), while TI-LVDS is §102(b) prior art.

As previously discussed, Exhibit 1106 (the TI-LVDS reference) is cited on the face of the '310 patent as prior art non-patent literature. (*See* Ex. 1101, '310 patent at 1.) TI-LVDS discloses the use of bi-directional LVDS digital serial

drivers and digital serial receivers. (*See* Ex. 1106, TI-LVDS at Fig. 1 (showing drivers and receivers on both the camera head and camera control unit); Ex. 1109, Grindon Decl. at ¶¶ 191-192.) In fact, the '310 patent references digital drivers and digital receivers manufactured by Texas Instruments that implement the LVDS standard. (*See, e.g.*, Ex. 1101, '310 patent at 6:49-55, 6:64-7:1, 7:64-8:3, 8:13-17, 8:51-57.) Figure 1 of TI-LVDS shows "a typical connection with LVDS drivers and receivers." (Ex. 1106, TI-LVDS at 6-7.) Thus, the use of LVDS for transmitting digital data was well-known prior to the alleged '310 patent invention. (*See* Ex. 1109, Grindon Decl. at ¶¶ 191-192.)

For the identical reasons discussed above in Ground 6 with respect to Nakamura, Okada, and Adler, it would have been obvious to utilize the LVDS communication protocol in TI-LVDS in the combination of Nakamura and Okada. Specifically, one of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system. (*See id.* at ¶¶ 193-194.) The combination would have involved the known method of simply replacing Nakamura/Okada's digital serial drivers and receivers with comparable LVDS modules. (*See id*.) The result would have been predictable; the resulting system would use LVDS serial communication protocol and LVDS drivers and receivers to transmit information. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. LVDS was an improved communication protocol because it was particularly appropriate for video applications, with higher data rates, lower power, and adaptability to lower voltages. (*See id.*) It would have been obvious to employ the high bit rate of the LVDS in Nakamura/Okada because a higher bit rate is more advantageous in video applications because it can transfer data more quickly. (*See id.*) LVDS would have improved the combination in the same way as the TI-LVDS reference. (*See id.*)

There are no secondary considerations of which Petitioner is aware that would tend to show that the combination of Nakamura, Okada, and TI-LVDS is non-obvious—particularly any secondary considerations having a nexus to the claimed invention. (*See id.* at ¶ 196.)

VI. REASONS WHY PROPOSED GROUNDS ARE NON-REDUNDANT

Eto and Nakamura are both primary references that disclose video imaging systems having most of the elements of the ‘310 patent claims. Eto and Nakamura, however, disclose the various ‘310 patent claim elements (such as the camera head, control unit, cable, serializer, digital serial driver, digital serial receiver, and analog-to-digital converter) in different ways and using different nomenclature.

Okada discloses the same type of video imaging system, but specifically for use in an endoscope. Okada also discloses interchangeable camera heads through the use of a processor and memory on the camera head. Adler and TI-LVDS are the only references disclosing LVDS communication protocol. Adler, however, is §102(e) prior art, while TI-LVDS is §102(b) prior art. King discloses yet another video imaging system, but provides more detailed disclosure of a timing signal generator and controlling the camera control unit in response to a timing signal.

Further, each of the grounds in this petition is non-redundant with a second petition filed on the same day by Petitioner asserting invalidity of claims 1-16, 19-22, 25, and 26 of the '310 patent. That petition raises an anticipation ground (whereas this petition raises only obviousness grounds), and it raises alternative obviousness grounds based on different primary references that are non-redundant.

VII. CONCLUSION

For the above reasons, Petitioner respectfully requests institution of *inter partes* review of claims 1-16, 19-22, 25, and 26 of the '310 patent.

Dated: February 19, 2015

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,471,310 and Exhibits 1101-1110 were served on February 19, 2015 by Federal Express on the following attorney of record listed on PAIR:

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