UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STRYKER CORPORATION,

Petitioner

v.

KARL STORZ ENDOSCOPY-AMERICA, INC.,

Patent Owner

Patent No. 7,821,530

Issue Date: October 26, 2010

Title: INTELLIGENT CAMERA HEAD

IPR Number 2015-00675

PETITION FOR *INTER PARTES* REVIEW

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Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Stryker Corporation ("Stryker" or "Petitioner") respectfully petitions for *inter partes* review ("IPR") of claims 1-6, 8-9 of U.S. Patent No. 7,821,530 ("the '530 patent"), which issued on October 26, 2010, and is assigned to Karl Storz Endoscopy-America, Inc. ("KSEA" or "Patent Owner").

I. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Stryker Corporation is the real party-in-interest. Stryker Communications, Inc., a wholly owned subsidiary of Stryker Corporation, is also an interested party.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

KSEA asserted the '530 patent against Stryker in the following patent infringement litigation: *Karl Storz Endoscopy-America, Inc. v. Stryker Corporation and Stryker Communications, Inc.*, Case No. 14-00876 (N.D. Cal.), filed February 26, 2014 ("the litigation"). KSEA served the complaint on Stryker no earlier than March 4, 2014. (Ex. 1110.) No patent applications are pending which claim priority to the '530 patent's application. Stryker has, however, filed a second IPR petition on the same day (IPR2015-00674), asserting invalidity of claims 1-6, 8-9 of the '530 patent. Stryker has also filed two IPR petitions on the same day on U.S. Pat. No. 7,471,310 (to which the '530 patent claims priority), which are IPR2015-00672 and IPR2015-00673. Stryker is also concurrently filing

petitions for *inter partes* review of the other three patents that KSEA asserted against Stryker in the litigation. (*See* IPR Nos. 2015-00764, 2015-00677, 2015-00678, 2015-00679.)

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel. Pursuant to 37 C.F.R. § 42.8(b)(4), a Power of Attorney accompanies this Petition. Lead Counsel: Robert A. Surrette (Reg. No. 52,262), bsurrette@mcandrews-ip.com. Back-up Counsel: Merle S. Elliott (Reg. No. 52,857), melliott@mcandrews-ip.com; and Christopher Scharff (Reg. No. 53,556), cscharff@mcandrews-ip.com. Post and Delivery: McAndrews, Held & Malloy, 500 West Madison St., 34th Floor, Chicago, IL 60662. Telephone: 312-775-8000. Facsimile: 312-775-8100.

D. Service Information Under 37 C.F.R. § 42.8(b)(4)

Please address all correspondence to the lead counsel at the address provided in Section I.C of this Petition. Petitioner also consents to electronic service by email at: StrykerKSIPR@mcandrews-ip.com.

II. PAYMENT OF FEES – 37 C.F.R. § 41.103

The required fee has been paid online. Please charge any fee deficiencies or credit any overpayments to Deposit Account No. 13-0017.

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R § 42.104

A. Grounds For Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that the '530 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the '530 patent.

B. Identification Of Challenge Under 37 C.F.R. § 42.104(b) And Relief Requested

Petitioner requests *inter partes* review of claims 1-6, 8-9 of the '530 patent on the grounds set forth below and requests that these claims be found unpatentable. An explanation of how claims 1-6, 8-9 are unpatentable under specified statutory grounds is provided below, including an identification of where each element is found in the prior art and the relevance of each reference. Additional explanation and support for this IPR and each ground of rejection is set forth in the Declaration of Dr. John R. Grindon, D. Sc. (Ex. 1109), which is submitted in accordance with 37 C.F.R. § 1.68. *Inter partes* review of claims 1-6, 8-9 is requested in view of the following references:[1]

- U.S. Patent No. 5,701,581 ("Eto") issued December 23, 1997, which is §102(b) prior art (Ex. 1103);

[1] The earliest claimed priority date for the '530 patent is December 28, 2001. Without agreeing that the patent claims are entitled to that priority date, for purposes of this IPR any dispute over the priority date does not matter, as each of the asserted references are prior art regardless.

- U.S. Patent No. 6,476,852 ("Okada") filed June 28, 1999, which is §102(e) prior art (Ex. 1104);
- U.S. Patent No. 6,659,940 ("Adler") filed April 5, 2001, which is §102(e) prior art (Ex. 1105);
- Texas Instruments Interface Circuits for TIA/EIA-644 LVDS Design Notes, Nov. 1998 ("TI-LVDS") (Ex. 1106), which is §102(b) prior art (Ex. 1106);
- U.S. Patent No. 6,608,647 ("King") filed May 29, 1998, which is §102(e) prior art (Ex. 1107); and
- U.S. Patent No. 4,996,975 ("Nakamura") issued March 5, 1991, which is §102(b) prior art (Ex. 1108).

Ground	Proposed Statutory Rejections for the '530 Patent
1	Claims 1-6 rendered obvious by Eto and Okada
2	Claims 8-9 rendered obvious by Eto, Okada, and Adler
3	Claims 8-9 rendered obvious by Eto, Okada, and TI-LVDS
4	Claims 1-6 rendered obvious by Eto, Okada, and King
5	Claims 1-6 rendered obvious by Nakamura and Okada
6	Claims 8-9 rendered obvious by Nakamura, Okada, and Adler
7	Claims 8-9 rendered obvious by Eto, Okada, and TI-LVDS

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

A claim subject to *inter partes* review is given its "broadest reasonable construction in light of the specification of the patent in which it appears," which may be a broader construction than applied by courts during claim construction.[2] *See* 37 C.F.R. § 42.100(b); *see also Corning Optical Comm. RF, LLC v. PPC Broadband, Inc.*, IPR2013-00340, Paper 79 (P.T.A.B. Nov. 21, 2014); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Further, "[c]onsistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning, as understood by a person of ordinary skill in the art, in the context of the entire patent disclosure." *AOL Inc. v. COHO Licensing, LLC*, IPR214-771, Paper 10 (P.T.A.B. Nov. 20, 2014).

Petitioner proposes the following claim constructions:

In independent claim 1, the claim preamble – **"*[a] video imaging system*"** – does not serve as a claim limitation. A preamble is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention. *See, e.g., Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1347 (Fed. Cir. 2012) ("[A]s a general rule preamble language is not treated as limiting."); *Marrin*

[2] Because of the different claim construction standard in litigation, Petitioner reserves all of its rights with regard to constructions during litigation.

v. Griffin, 599 F.3d 1290, 1294 (Fed. Cir. 2010) ("Preamble language that merely states the purpose or intended use of an invention is generally not treated as limiting the scope of the claim.") Because "[a] video imaging system" does not recite essential structure, it is not limiting. (*See* Ex. 1109, Grindon Decl. at ¶ 25.)

In independent claim 1, "***camera head***" is "a device that generates an uninterrupted sequence of data that represents moving visual images." The remainder of claim 1 recites that the camera control unit is coupled to the camera head and processes a stream of digital video data. (Ex. 1001, '530 patent at claim 1.) Therefore, the camera head must be a device that generates an uninterrupted (i.e., continuous) sequence of data (i.e., stream of data) that represents moving visual images (i.e., video). (*See* Ex. 1109, Grindon Decl. at ¶ 26.)

Moreover, the "***camera head***" in claim 1 is not limited to an endoscopic video camera. (*See id.* ¶ 27-36.) First, an "endoscope" is simply not a limitation of any claim. *See, e.g., Johnson Worldwide Assoc., Inc. v. Zebco, Corp.*, 175 F.3d 985, 989 (Fed. Cir. 1999) ("general descriptive terms will ordinarily be given their full meaning; modifiers will not be added to broad terms standing alone"). Second, the broadest reasonable construction of camera head is not an endoscopic video camera, as that would be a much narrower construction limiting the claim to a specific type of camera head. And during prosecution of the related U.S. Pat. No. 7,471,310 (from which the '530 patent is a continuation), the Examiner rejected

pending claims reciting a "camera head" as anticipated and obvious in view of numerous prior art references that were not directed to endoscopes, and the applicants never argued that those rejections were improper because the references lacked disclosure of an endoscopic video camera. (*See* Ex. 1111, '310 patent Prosecution History at 241-242, 255, 267-268, 294, 313-314.)

The remaining terms should receive their broadest reasonable construction.

IV. BACKGROUND OF THE '530 PATENT

The '530 patent generally relates to a video imaging system with interchangeable camera heads. (*See* Ex. 1109, Grindon Decl. at ¶¶ 17-22; Ex. 1101, '530 patent at Abstract.) The focus of the '530 is the ability for a single camera control unit to control multiple different types of camera heads. (*See id.*)

The '530 patent purports to disclose, in independent claim 1, a video imaging system including a camera control unit, a cable, and a camera head. *See* Ex. 1101, '530 patent at claims.) The camera head including an imager, a digital driver, a processor, and a memory accessible by the process and containing camera head information. (*See id.*) The camera control unit processes a continuous stream of digital video data, and also includes a digital serial receiver and a plurality of camera heads are attachable to and controlled by the camera control unit. (*See id.*) Dependent claim 2 includes a timing generator in the camera head. (*See id.*) Dependent claim 3 includes a timing signal sent to the camera control unit. (*See*

id.) Dependent claim 4 includes a converter for converting the analog image signal to a digital signal. (*See id.*) Dependent claim 5 includes a multiplexer for generating a multiplexed signal. (*See id.*) Dependent claim 6 includes a serializer for serializing the image signal. (*See id.*) Dependent claims 8 and 9 relate to the use of LVDS. (*See id.*)

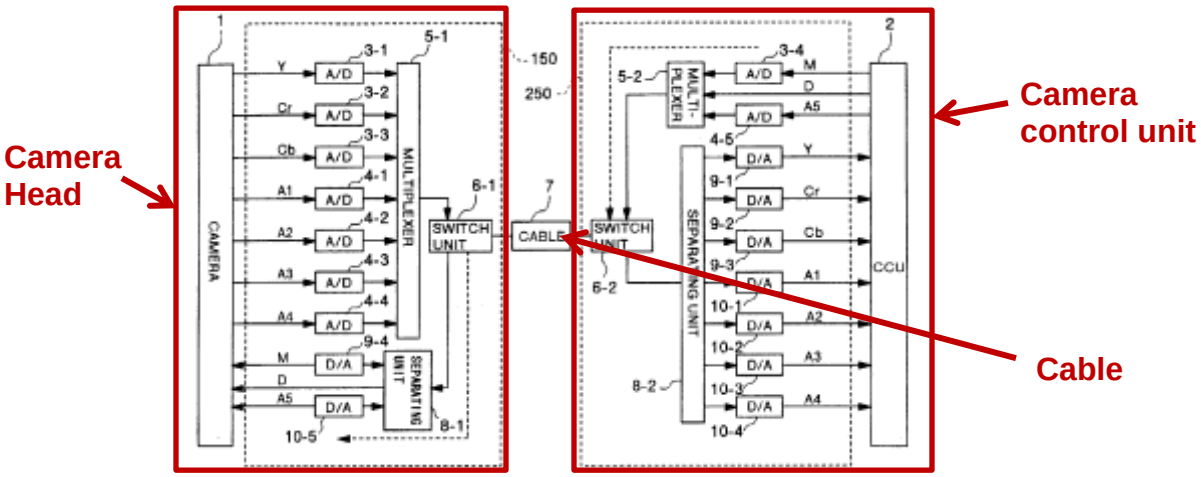
V. ELEMENT-BY-ELEMENT ANALYSIS OF HOW CHALLENGED CLAIMS ARE UNPATENTABLE (37 C.F.R. §§42.104)

There is a reasonable likelihood that claims 1-6, 8-9 are unpatentable because they are rendered obvious in view of the prior art.

A. Ground 1: Claims 1-6 are Obvious Under 35 U.S.C. § 103(a) by Eto and Okada (Processor and Memory Reference)

Claims 1-6 are obvious under 35 U.S.C. § 103(a) in view of Eto in combination with Okada.

Eto discloses a general video imaging system that comprises a camera control unit, a cable, and a camera head, as shown below:



(Ex. 1103, Eto at Fig. 1 (annotated).) The camera head of Eto includes an imager, a timing generator, a converter, a serializer, a digital driver, a digital serial receiver, a multiplexer, and a processor. The camera control unit of Eto includes a digital serial receiver and a digital receiver that is controlled based in part upon the timing signal. Okada, meanwhile, also discloses a video imaging system having a camera head and a camera control unit. The camera head of Okada, however, includes a processor and memory containing information about the camera head. The memory of Okada is accessible to the processor.

For the reasons discussed below, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention of the '530 patent to include a processor and memory in the camera head of Eto, as taught by Okada. Such a combination satisfies all of the elements of claims 1-6.

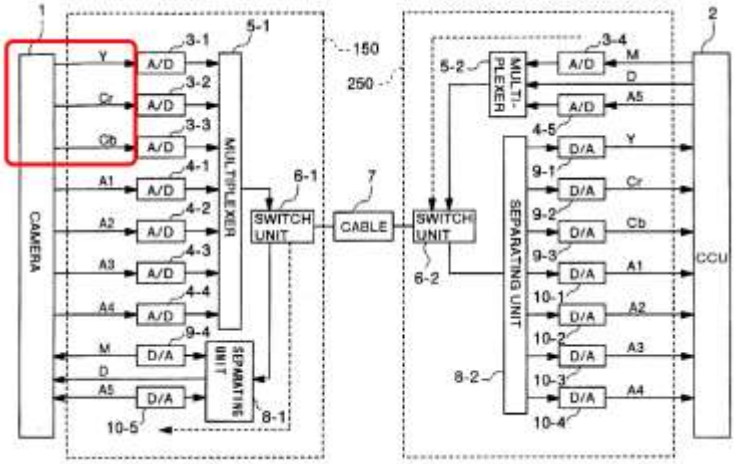
(i) Independent claim 1

First, to the extent the preamble is limiting, Eto discloses a "*video imaging system*." (*See* Ex. 1103, Eto at 13:47-49, 1:8-14 ("[t]he present invention relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU', i.e., Camera Control Unit) are coupled with each other. . . .").) (*See also* Ex. 1109, Grindon Decl. at ¶ 50.)

Second, Eto discloses a "*camera head*." Eto describes "television camera 1" that obtains a "video signal." (Eto at 7:7-19.) Figure 1 (shown above) illustrates

the "camera" connected to the cable. (*Id.* at Fig. 1) (*See also* Ex. 1109, Grindon Decl. at ¶ 51.)

Third, Eto discloses that the camera head includes "*an imager generating a stream of video data*." Figure 1 of Eto shows the imager (i.e., the Y, Cr, and Cb analog video components of the camera together with the corresponding A/D converters 3-1, 3-2, and 3-3):



(Ex. 1103, Eto at Fig. 1 (annotated).) Further, Eto states that this imager is for generating a stream of video data. It states that "a video (picture) signal obtained from a television camera 1 is three sorts of video signals, i.e., a luminance signal 'Y' and two sorts color difference signals 'Cr' and 'Cb' instead of the respective video signals R, G, B." (Ex. 1103, Eto at 7:7-19 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 52.)

Fourth, Eto discloses that the camera head includes "*at least one digital driver*." Eto discloses transmitting a serial signal over cable 110 to the CCU 118

side. The structure in Eto that drives the digital serial signal (and thus is the "digital driver") is the "data output gate 120." (*See* Ex. 1109, Grindon Decl. at ¶ 53.) Alternatively, one of ordinary skill in the art at the time of the alleged invention would have known that transmitting a serial digital signal over a cable must necessarily and inherently involve a driver to drive the signal. (*See id.*)

Fifth and Sixth, "*a processor*" and "*a memory device, accessible by said processor, containing camera head information*" in the camera head are found in the combination of Eto and Okada. (*See also* Ex. 1109, Grindon Decl. at ¶¶ 54-55.) Okada discloses a "first CPU" on the "scope side" (i.e., camera head). (Ex. 1104, Okada at 4:4-15.) The CPU "controls the total" of the timing circuits and switching. (*Id.*) Okada discloses a "ROM" memory on the "scope side." (Ex. 1104, Okada at Fig. 1.) Okada discloses "to the first CPU 20 [on the camera head] a ROM 21 storing setting data . . . is connected." (*Id.* at 4:16-28.) Okada discloses that "the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit . . ." (*Id.* at 4:58-5:3.)

It would have been obvious in view of Okada to provide a processor on the camera head and a memory on the camera head in Eto, to enable the use of different camera heads. (*See* Ex. 1109, Grindon Decl. at ¶ 56.) Among other reasons, the combination would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use

of prior art elements according to their established functions. (*See id.*) Specifically, including a processor with access to a memory in the camera head would be advantageous because such a processor and memory would allow for local processing and use of the information in the memory. (*See id.*) One of ordinary skill in the art would have looked to other video imaging systems, including in the field of endoscopes, to conclude that a processor on the camera head would be an obvious way to implement interchangeable camera heads. (*See id.*) At the time of the alleged invention of the '530 and '530 patents, the advantages of interchangeable camera heads were well-known. (*See id.*) It would have been obvious to employ the processors and memory including information about the camera head in a video imaging system because interchangeability of camera heads would have been advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*)

Seventh, Eto discloses "*a cable*." Eto discloses a "cable" in, for example, Figure 1. (*See* Ex. 1103, Eto at Fig. 1.) Eto also discloses that "digital signals are transmitted via the cable in the digital code form." (Ex. 1103, Eto at 3:43-48.) (*See also* Ex. 1109, Grindon Decl. at ¶ 57.)

Eighth, Eto discloses "*a camera control unit coupled to said camera head via said cable*." Eto discloses that it "relates to an apparatus such that two video

appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU,' i.e., Camera Control Unit) are coupled with each other by employing a single transmission path through which a video signal, an audio signal, and a control signal are multiplexed and transmitted in a bidirectional manner." (Ex. 1103, Eto at 1:8-14 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 58.)

Ninth, Eto discloses that the camera control unit has "*at least one digital receiver*." This limitation is satisfied by the "data fetching gate 121" of Eto, which receives the digital serial data signal. (Ex. 1109, Grindon Decl. at ¶ 59.) Alternatively, this limitation is simply inherent in Eto by virtue of its disclosure of transmitting digital serial information over a cable from a camera to a control unit. One of ordinary skill in the art would have known that transmitting a serial digital signal over a cable necessarily and inherently requires a digital serial receiver to receive the digital serial signal that is transmitted. (*See id.* at ¶ 59.)

Tenth, Eto discloses the "*camera control unit processing a stream of digital video data*." (*See* Ex. 1109, Grindon Decl. at ¶¶ 60-61.) Again, Eto discloses that it "relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU,' i.e., Camera Control Unit) are coupled with each other by employing a single transmission path through which a video signal, an audio signal, and a control signal are multiplexed

and transmitted in a bidirectional manner." (Ex. 1103, Eto at 1:8-14 (emphasis added).) The camera control unit therefore processes the digital video data produced by the camera head. (*See* Ex. 1109, Grindon Decl. at ¶ 60.)

Eleventh, the combination of Eto and Okada discloses "*a plurality of camera heads are attachable to and controlled by said camera control unit*." (*See* Ex. 1109, Grindon Decl. at ¶¶ 62-64.) Okada provides for the interchangeability of two different types of cameras having differing timing signals, i.e., NTSC and PAL. (Ex. 1104, Okada at 6:10-19.) Further, for the reasons discussed above, adding a memory and processor in a camera head to Eto from Okada would have enabled interchangeable camera heads. (*See supra*.) Interchangeable camera heads would have been advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Providing interchangeable camera heads to the imaging system of Eto would have involved merely the use of a known technique to improve a similar system in the same way, and/or the predictable use of prior art elements according to their established functions. (*See id.*)

(ii) Claim 2:

Eto in combination with Okada satisfies the requirement that "s*aid camera head further comprises a timing generator for generating a timing signal particular to said camera head, wherein the timing signal actuates said imager*."

(*See* Ex. 1109, Grindon Decl. at ¶ 66.) This element is disclosed in Okada, which describes "on the scope side" a "timing generator 16." (Ex. 1104, Okada at 4:4-15, Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35 ("In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525).") The timing signal of Okada thus actuates the imager and is sent to the camera control unit. (*See* Ex. 1109, Grindon Decl. at ¶ 66.)

It would have been obvious in view of Okada to provide a timing generator particular to the camera head to actuate the imager. (*See id.* at ¶ 67.) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) Specifically, using the known method of Okada to including the timing signal generator in the camera head, and sending that timing signal to the camera control unit would have enabled interchangeable camera heads, with synchronization of the camera head and camera control unit. (*See id.*) A camera head that generates a timing signal that is sent to the camera

control unit and used to control the camera control unit would predictably allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*)

(iii) Claim 3:

The combination of Eto and Okada discloses that "*the timing signal is sent to said camera control unit*." (*See* Ex. 1109, Grindon Decl. at ¶ 68.) (*See* Ex. 1104, Okada at 4:4-15, Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35 ("In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525).").) Okada states that "In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20,

either of the oscillators 17, 18 is selected." (Ex. 1104, Okada at 4:5-15.)

The timing generator 16 is in the camera head, and the imaging memory 24A is in the camera control unit. (*See* Ex. 1109, Grindon Decl. at ¶ 68.) In order for the picture data to be written into the imaging memory "in the timing of the synchronization signal formed in the timing generator 16," the synchronization signal must be sent to the camera control unit which contains the imaging memory. (*See id.*) Okada further states that "the picture signal obtained in this CCD 1 is supplied to the memory section 24 on the processor side through the AGC circuit 5 including the correlative double sampling processing and the DSP circuit 22 similarly to the above. In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal of the PAL system formed in the timing generator 16, that is, by the horizontal synchronization signal." (Ex. 1104, Okada at 5:48-56). Thus, as disclosed by Okada, the timing generator 16 in the camera head (scope side) must send a timing synchronization signal to the CCU (processor side), used to write the transferred picture data into memory 24 on the camera control unit, or CCU. (*See id.*) In other words, the timing signal is sent to the camera control unit.

Including the timing signal generator in the camera head and sending that timing signal to at least partially control the camera control unit would have been obvious because such a timing signal would allow for the interchangeability of

camera heads and synchronization of the camera head and camera control unit. (*See id.* at ¶ 69.) Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*) Interchangeable camera heads would be useful to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Providing this feature would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*)

(iv) Claim 4

Eto discloses that "*said imager produces analog image data and said camera head further comprises a converter for converting the analog image signal to a digital image signal*." (*See* Ex. 1109, Grindon Decl. at ¶ 70.) Eto states that on the camera head, the "analog video signals are A/D-converted by A/D converters 3-1, 3-2, 3-3 of a transmitting/receiving apparatus 150 into digital video signals." (Ex. 1103, Eto at 7:7-19 (emphasis added).) The A/D converters are shown in Figure 1 of Eto. (Ex. 1103, Eto at Fig. 1.)

(v) Claim 5

Eto discloses that "*said camera head further comprises a multiplexer for generating a multiplexed signal, wherein the multiplexed signal includes the image signal and control signals*." (*See* Ex. 1109, Grindon Decl. at ¶ 71.) Eto states that "The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are multiplexed in the time-divisional multiplexing circuit 102, are compressed with respect to the time axis in time axis compressing circuit 103, and thereafter are converted into serial data by parallel-to-serial converting circuit 104." (Ex. 1103, Eto 581 at 15:6-11.)

(vi) Claim 6

Eto also discloses that "*said camera head further comprises a serializer for serializing the image signal*." (*See* Ex. 1109, Grindon Decl. at ¶ 72.) Eto describes that "[t]he camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals . . . are converted into serial data by parallel-to-serial converting circuit 104. Thus, the resultant serial data constitute the transmission signal on the camera side, as represented in FIG. 12. The transmission signal is transmitted via a cable 110 to the CCU 118 side." (Eto at 15:6-15 (emphasis added).) In other words, the parallel-to-serial converting circuit is a "serializer for serializing the image signal."

(vii) Lack of Secondary Considerations

There are no secondary considerations of which Petitioner is aware that

would tend to show that the combination of Eto and Okada is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 73.)

(viii) Claim Charts

The below claim charts contain detailed citation to disclosure in Eto and Okada that discloses each element of claims 1-6 of the '530 patent.

'530 Patent Claim 1	**Eto in Combination With Okada**
1. A video imaging system comprising:	Ex. 1103, Eto at 1:8-14 ("The present invention relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU', i.e., Camera Control Unit) are coupled with each other by employing a single transmission path through which a video signal, an audio signal, and a control signal are multiplexed and transmitted in a bidirectional manner."), 7:7-9, 13:47-49, Figs. 1, 11. Ex. 1104, Okada 852 at 3:58-61 ("FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention."), 1:12-16, Fig. 1.)
a camera head	Ex. 1103, Eto '581 at 7:7-19 ("In FIG. 1, there is shown an arrangement of a video (picture) signal bidirectional transmission system according to an embodiment of the present invention. . . . . These three sorts of analog video signals are A/D-converted by A/D/ converters 3-1, 3-2, 3-3 of a transmitting/receiving apparatus 150 into digital video signals."), Figs. 1, 11.) Ex. 1104, Okada '852 at 4:4-15 ("In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having . . . CCD 1. . . Furthermore, a first CPU 20 is provided, which controls the total while

	controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected.").)
including an imager generating a stream of video data,	Ex. 1103, Eto '581 at 7:7-19 ("In FIG. 1, there is shown an arrangement of a video (picture) signal bidirectional transmission system . . . a video (picture) signal obtained from a television camera 1 is three sorts of video signals, i.e., a luminance signal 'Y' and two sorts color difference signals 'Cr' and 'Cb'. . . . These three sorts of analog video signals are A/D-converted by A/D converters . . . into digital video signals."), Figs. 1, 11.) Ex. 1104, Okada '851 at 4:4-15, Fig. 1.
at least one digital driver,	Ex. 1103, Eto '581 at 15:6-15 ("The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are . . . converted into serial data by parallel-to-serial converting circuit 104. Thus, the resultant serial data constitute the transmission signal on the camera side, as represented in FIG. 12. The transmission signal is transmitted via a cable 110 to the CCU 118 side."), 16:44-48 ("data output gate 120").
a processor,	Ex. 1104, Okada '852 at 4:4-15 ("[A] first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected."), Fig. 1.
and a memory device, accessible by said processor, containing camera head information;	Ex. 1104, Okada 852 at 4:16-28 ("[T]o the first CPU 20, a ROM 21 storing setting data for the control meeting the NTSC system or the PAL system is connected."), Fig. 1, 4:58-5:3 ("the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set"), 4:4-15, Okada at 4:16-28 ("ROM 21 stor[es] setting data for the control meeting the NTSC system or the PAL system [and] is connected . . to the first CPU 20 [on the camera head]."), 4:58-5:3 ("the selected setting data is read out from the

	ROM 21 by the first CPU 20 to set the processing contents of each circuit . . .")
a cable; and	Ex. 1103, Eto '581 at 3:43-48 ("these digital signals are transmitted via the cable in the digital code form."), at 7:66-8:4 (digital video signals generated by the camera head are received by "transmitting/receiving apparatus 250 employed on the side of the CCU 2 . . . from the cable 7"), Figs. 1, 11.
a camera control unit coupled to said camera head via said cable	Ex. 1103, Eto '581 at 1:8-14 ("The present invention relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU,' i.e., Camera Control Unit) are coupled with each other by employing a single transmission path through which a video signal, an audio signal, and a control signal are multiplexed and transmitted in a bidirectional manner.""), 4:44-53, 4:54-57, 7:66-8:4 (digital video signals are received by "transmitting/receiving apparatus 250 employed on the side of the CCU 2 . . . from the cable 7") Ex. 1104, Okada '852 at 4:34-40 ("external processor side")
and having at least one digital receiver;	Ex. 1103, Eto '581 at 15:6-15 ("The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are . . . converted into serial data by parallel-to-serial converting circuit 104. Thus, the resultant serial data constitute the transmission signal on the camera side, as represented in FIG. 12. The transmission signal is transmitted via a cable 110 to the CCU 118 side."), 16:36-43 ("data fetching gate 121"), Fig. 11.
said camera control unit processing a stream of digital video data;	Ex. 1103, Eto at 1:8-14 ("The present invention relates to an apparatus such that two video appliances such as a television camera and a controlling unit thereof (will be referred to a 'CCU,' i.e., Camera Control Unit) are coupled with each other by employing a single

	transmission path through which a video signal, an audio signal, and a control signal are multiplexed and transmitted in a bidirectional manner."), 4:44-53, 4:54-57, 7:66-8:4. Ex. 1104, Okada at 4:34-40 ("external processor side").
wherein a plurality of camera heads are attachable to and controlled by said camera control unit.	Ex. 1104, Okada '852 at 4:58-5:3 ("[T]his second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set."), 5:21-35, Fig. 1, 4:58-5:20, 6:10-19 ("Thus, in this example, it is possible to form and display both the picture data of the NTSC system and the picture data of the PAL system by using the CCD 1 for the NTSC system. Furthermore, in the above example, it is also possible to form and display the pictures of both systems by the processing similar to that of the above, by using a CCD 1 suitable for the scanning line of the PAL system, and furthermore, it is also possible to use a CCD for the PAL as an imaging element, and the scanning line change circuit in that case is made to perform the compression action.")
'530 Patent, Claim 2	**Eto in Combination With Okada**
2. The video imaging system according to claim 1 wherein said camera head further comprises a timing generator for generating a timing signal particular to said camera head, wherein the timing	Ex. 1104, Okada '852 at 4:4-15 ("In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU

signal actuates said imager.	20, either of the oscillators 17, 18 is selected."), Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35 ("In this memory section 24, the picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B (as the data corresponding to the number of scanning lines of 525)."), 5:48-56.
'530 Patent, Claim 3	**Eto in Combination With Okada**
3. The video imaging system according to claim 2 wherein the timing signal is sent to said camera control unit.	Ex. 1104, Okada '852 at 4:58-5:3 ("[T]his second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set."), 5:21-35 ("picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B. . . . Then, each of these signals of R, G, and B is outputted to a monitor . . ."), Fig. 1, 4:58-5:20.
'530 Patent, Claim 4	**Eto in Combination With Okada**
4. The video imaging system according to claim 1 wherein said imager produces analog image data and said camera head further comprises a converter for	Ex. 1103, Eto '581 at 7:7-19 ("These three sorts of analog video signals are A/D-converted by A/D converters 3-1, 3-2, 3-3 . . . into digital video signals."), Figs. 1 and 11.) Ex. 1104, Okada '852 at 4:29-33 ("[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5,

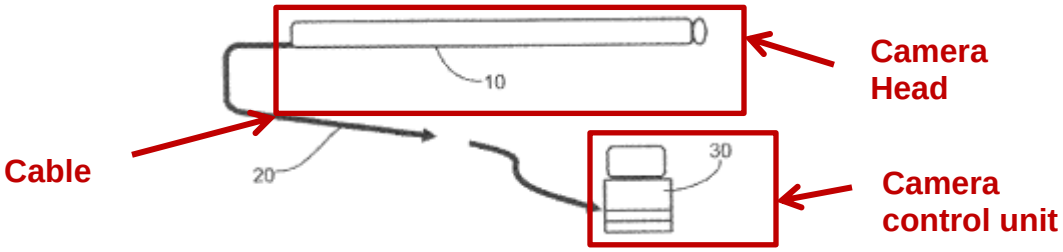
converting the analog image signal to a digital image signal.	a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6.")
'530 Patent, Claim 5	**Eto in Combination With Okada**
5. The video imaging system according to claim 1 wherein said camera head further comprises a multiplexer for generating a multiplexed signal, wherein the multiplexed signal includes the image signal and control signals.	Ex. 1103, Eto 581 at 15:6-11 ("The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are multiplexed in the time-divisional multiplexing circuit 102, are compressed with respect to the time axis in time axis compressing circuit 103, and thereafter are converted into serial data by parallel-to-serial converting circuit 104."), 14:50-58.
'530 Patent, Claim 6	**Eto in Combination With Okada**
6. The video imaging system according to claim 1 wherein said camera head further comprises a serializer for serializing the image signal.	Ex. 1103, Eto '581 at 15:6-15 ("The camera 101 outputs the digitalized video signal, audio signal and control signal. These digitalized signals are . . . converted into serial data by parallel-to-serial converting circuit 104. Thus, the resultant serial data constitute the transmission signal on the camera side, as represented in FIG. 12. The transmission signal is transmitted via a cable 110 to the CCU 118 side.")

B. Ground 2: Claims 8-9 Are Obvious in View of Eto, Okada (Processor and Memory Reference) and Adler (LVDS Reference)

Claim 8 requires that *"the digital driver [on the camera head] utilizes Low-Voltage Differential Signals*." (Ex. 1101, '530 patent at claim 8.) Claim 9 similarly requires that "*the digital receiver [on the camera control unit] utilizes Low-Voltage Differential Signals*." (Ex. 1101, '530 patent at claim 9.) As discussed

above, Eto in combination with Okada would have rendered obvious all of the features of independent claim 1, including the use of a digital driver on the camera head and a digital receiver on the camera control unit. It would have been further obvious in view of Adler to use Low Voltage Differential Signals (LVDS) in such a video system, which would have satisfied claims 8-9.

Specifically, Adler teaches a video imaging system for an endoscope, comprising a camera head, camera control unit, and cable, as shown below:



(Ex. 1105, Adler at Fig. 1 (annotated), 9:24-38; Ex. 1109, Grindon Decl. at ¶ 76.) Just like Eto and Okada, the camera control unit of Adler processes a continuous stream of digital video data from the camera head, through the cable. (*See*, *e.g.*, Ex. 1105, Adler 940 at 9:24-33 ("The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope.") (emphasis added); *see also id.* at 9:39-47, 5:21-23 ("Preferably, the dedicated image processor is a motion video processor . . . .")

Adler, however, states that it specifically uses LVDS data transmission.

Adler states that "[t]he electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Ex. 1105, Adler 940 at 10:7-19 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 77.) One of ordinary skill in the art would have recognized that LVDS is an alternative communications protocol that is particularly appropriate for video applications because it has a high bit rate, lower power consumption, and can utilize lower voltages. (*See* Ex. 1109, Grindon Decl. at ¶ 78.)

It would have been obvious to employ the high bit rate LVDS protocol in the video imaging system of Eto in combination with Okada. Among other reasons, the combination would have been obvious because it involved merely the combination of known elements to achieve a predictable result. (*See* Ex. 1109, Grindon Decl. at ¶ 79.) One of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system). (*See id.*) Thus, one of ordinary skill in the art would have easily incorporated Adler's LVDS components in Eto's camera head and control unit because Eto already discloses that digital serial data is transmitted using drivers and receivers. (*See id.*) The result would be predictable; that is, the resulting video imaging system would

merely use a different communication protocol to transmit information between the camera head and camera control unit. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. (See Ex. 1109, Grindon Decl. at ¶ 80.) LVDS is particularly appropriate for video applications due to high data rates, lower power, and adaptability to lower voltages. (*See id*.) It would have been obvious to employ the high bit rate of LVDS in the video imaging system of Eto/Okada because a higher bit rate is more advantageous in video applications because it can transfer data more quickly. (*See id.*) LVDS would have improved the combination of Eto and Okada by providing the same benefits as in Adler. (*See id*.)

Additionally, the combination would have been obvious because Adler itself explicitly contains a teaching, suggestion, and motivation to to use LVDS in an endoscopic system. (*See* Ex. 1109, Grindon Decl. at ¶ 81; Ex. 1105, Adler at 10:7-19 (disclosing LVDS).) One of ordinary skill in the art would have read that disclosure in Adler as a motivation to LVDS in the Eto/Okada endoscopic video imaging system (*See* Ex. 1109, Grindon Decl. at ¶ 81.)

There are no secondary considerations of which Petitioner is aware that

would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 82.)

C. Ground 3: Claims 8-9 Are Obvious In View of Eto, Okada, and TI-LVDS (LVDS Reference II)

As discussed above in Ground 2, it would have been obvious at the time of the alleged invention of the '530 patent to substitute LVDS as the digital serial communication protocol in the combination of Eto and Okada. In Ground 2, Petitioner relied on Adler for disclosure of LVDS in a camera system very similar to those of Eto and Okada. Adler, however, is prior art under 35 U.S.C. §102(e). Should the Board determine that Patent Owner KSEA is able to swear behind Adler as prior art, there are numerous other §102(b) prior art references disclosing LVDS as a serial communication protocol, including the TI-LVDS reference. Accordingly, Ground 3 is non-redundant to Ground 2, because Ground 3 relies on §102(b) prior art for LVDS instead of §102(e) prior art.

The LVDS standard, formally known as TIA/EIA-644 Low-Voltage Differential Signaling, was created by Texas Instruments as "a signaling method used for high-speed, low-power transmission of binary data over copper." (Ex. 1106, TI-LVDS at 6.) Exhibit 1006 (the TI-LVDS reference) is cited on the face of the '5300 patent as prior art non-patent literature. (*See* Ex. 1101, '530 patent at 2.) In fact, the '530 patent references digital serial drivers and digital serial receivers manufactured by Texas Instruments that implement the LVDS standard.

(*See, e.g.*, Ex. 1101, '530 patent at 6:56-61.) Figure 1 of TI-LVDS shows "a typical connection with LVDS drivers and receivers." (Ex. 1106, TI-LVDS at 6-7.) Thus, the use of LVDS for transmitting digital data was well-known prior to the alleged '530 patent invention. (*See* Ex. 1109, Grindon Decl. at ¶¶ 85-91.)

For reasons similar to those discussed above with respect to Eto, Okada, and Adler, it would have been obvious to utilize the LVDS communication protocol in TI-LVDS in the combination of Eto and Okada. One of ordinary skill in the art would have recognized the benefits of LVDS as disclosed in TI-LVDS, such as very high bit rates (655 Mbit/s), low power consumption, and adaptability to low voltage levels, all of which are particularly suitable for small imaging devices, such as endoscopes. (*See id.*) The combination would involve the known method of simply replacing Eto/Okada's digital serial drivers and receivers with comparable LVDS modules. (*See* Ex. 1109, Grindon Decl. at ¶ 92.) The result would have been predictable; that is, the resulting video imaging system would merely use a different serial communication protocol to transmit information between the camera head and camera control unit. (*See id.*) One of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system). (*See id.* at ¶ 92.)

Alternatively, the combination would have been obvious because it results

from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. As explained above, LVDS would have improved the Eto/Okada system by providing for a higher bit rate that would allow the transmission of high resolution endoscopic video images. (*See id*. at ¶¶ 92-93.) LVDS would have improved the combination in the same way as the TI-LVDS reference. (*See id.*)

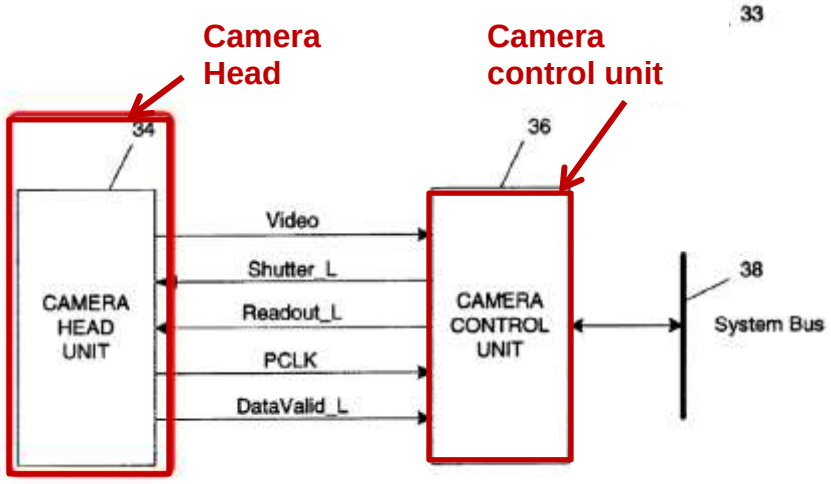
There are no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 94.)

D. Ground 4: Claims 1-6 Are Obvious Under 35 U.S.C. §103(a) in View of Eto, Okada (Processor and Memory Reference) and King (Timing Signal Reference)

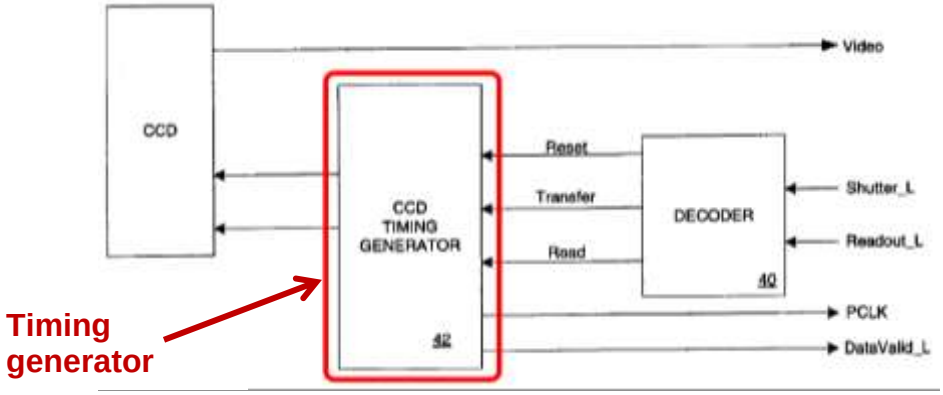
As discussed above, Eto in combination with Okada would have rendered obvious all of the features of claims 1-6. Even if Eto and Okada, did not disclose the claimed "*plurality of camera heads . . . attached to and controlled by said camera control unit*," as required by claim 1, the "*timing generator, for generating a timing signal particular to said camera head, wherein the timing signal actuates said imager*" of claim 2, or that "*the timing signal is sent to said camera control unit*" as recited by claim 3, however, these features were obvious in view of King.

King discloses a video imaging system including a camera head (34) and a

camera control unit (36), as shown below:



(Ex. 1107, King at Fig. 1 (annotated).) The camera head includes a CCD image sensor and a CCD timing generator (42):



(Ex. 1107, King at Fig. 2 (annotated) and 5:51-58.) The CCD Timing Generator 42 generates a "sequence of vertical and horizontal clock cycles required to completely transfer the image residing in the readout cells to the Camera Control Unit (CCU) 36." (Ex. 1107, King at 8:4-7.) Thus, King's CCD Timing Generator 42 is a "*timing generator, for generating a timing signal particular to said camera head, wherein the timing signal actuates said imager*," as required by claim 2.

(*See* Ex. 1109, Grindon Decl. at ¶¶ 97-98.)

King also explains that "[a]long with the image signal, the CHU 34 returns a clocking signal, PCLCK, that indicates the timing of the video signal and a data valid signal, DATA VALID_L, identifying that portion of the video signal containing valid image data." (Ex. 1107, King at 6:8-12.) The PCLCK signal is a "pixel clock," for clocking pixels in the video signal sent to the CCU from the CHU, and is generated by the same timing and control unit (the "CCD Timing Generator") that drives the imager. (Ex. 1107, King at Figs. 2, 3; *see also id.* at 6:37-40.) King further explains that "[t]he final step [to acquire an image from the CCD imager is] to move or output the charges to the Camera Head Unit, which combines them with timing information to form an image signal for application to the Camera Control Unit (CCU)." (*Id.* at 5:9-12 (emphasis added).) Thus, the timing signal generated by King's CCD Timing Generator 42 is also "sent to said camera control unit." Therefore, King discloses that "*the timing signal is sent to said camera control unit*" as recited by claim 3. (Ex. 1109, Grindon Decl. at ¶ 99.)

This timing generator in King, in turn, allows King to provide a number of different camera heads, each controllable by a single camera control unit. King states that "[s]ince a single Camera Control Unit (CCU) 36 preferably supports configurations with multiple Camera Head Units (CHUs), a set of shutter (C0 Shutter_L . . . Cn Shutter_L) and readout (C0 Readout_L . . . Cn Readout_L)

controls are derived for each potentially installed CHU." (Ex. 1107, King at 6:47-51.) (Ex. 1109, Grindon Decl. at ¶ 99.) Therefore, King discloses a "*plurality of camera heads . . . attached to and controlled by said camera control unit*."

It would have been obvious to one of ordinary skill in the art to combine Eto, Okada, and King because the combination would involve substitution of one known element for another to obtain predictable results. (Ex. 1109, Grindon Decl. at ¶ 101.) As previously explained, the combination of Eto and Okada discloses each and every element of claims 1-6. (*See id.*) King discloses a timing generator in the camera head also. In King, CCD Timing Generator 42 actuates the imager and transmits pixel clock (PCLK) to the CCU for synchronization. Moreover, adding King's timing generator to the system would create an alternative means of communicating the video signal to the CCU by enabling the CCU to synchronize the data signals using the timing signal actuating the imager. Thus, transmitting the timing and/or data signals to the CCU would predictably result in an alternative means of sending timing data to the CCU.

Additionally, it would have been obvious to one of ordinary skill in the art to combine Eto, Okada, and King because the combination would involve applying a known technique to a known device ready for improvement to yield a predictable result. (Ex. 1109, Grindon Decl. at ¶ 102.) Specifically, King discloses the use of multiple camera heads, which could be of different types because each is provided

with its own set of timing and control signals. (*See* Ex. 1107, King at 6:47-55.) Allowing the camera head to generate a timing signal that is sent directly to the CCU and used to control the CCU would enable the camera head and CCU to remain synchronized, even if the CCU interoperates with a plurality of different camera heads. Thus, King discloses a known technique that enables the interchangeability of camera heads. This is because the information needed by the camera control unit to operate with a particular one of the different types of camera heads is stored on the camera head itself, and so when another camera head is plugged into the camera control unit the camera head information for that camera head is provided to the camera control unit so that it can adapt to and operate properly with the synchronization and timing requirements of that particular camera head. (Ex. 1109, Grindon Decl. at ¶ 102.)

There are no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 104.)

E. Ground 5: Claims 1-6 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura and Okada (Processor and Memory Reference)

Claims 1-6 are also obvious under 35 U.S.C. § 103(a) in view of Nakamura in combination with Okada. Similar to Eto, Nakamura discloses a video imaging system that comprises a camera control unit, a cable, and a camera head. The

camera head of Nakamura includes an imager, a timing generator, a converter, a serializer, a digital serial driver, a multiplexer, and a processor. And the camera control unit of Nakamura includes a digital serial receiver that is controlled based at least in part upon the timing signal. Nakamura is non-redundant with Eto because Nakamura contains different disclosure regarding the claimed features.

Okada, meanwhile, again also discloses a video imaging system including a camera head and a camera control unit. The camera head of Okada, however, includes a processor and memory containing information about the camera head, and the memory is accessible to the processor. Further, Okada expressly discloses that the video imaging system can be used in an endoscope.

For the reasons below, it would have been obvious to a person of ordinary skill in the art at the time of the invention of the ‘530 patent to include a processor and memory in the camera head of Nakamura, as taught by Okada. Such a combination would satisfy all of the elements of claims 1-6.

(i) Independent claim 1

All of the elements of independent claim 1 are found in the combination of Nakamura and Okada. First, to the extent the preamble is limiting, Nakamura discloses a “*video imaging system*.” Nakamura’s video imaging system comprises a camera, a cable, and a camera control unit, as shown below in Fig. 1:

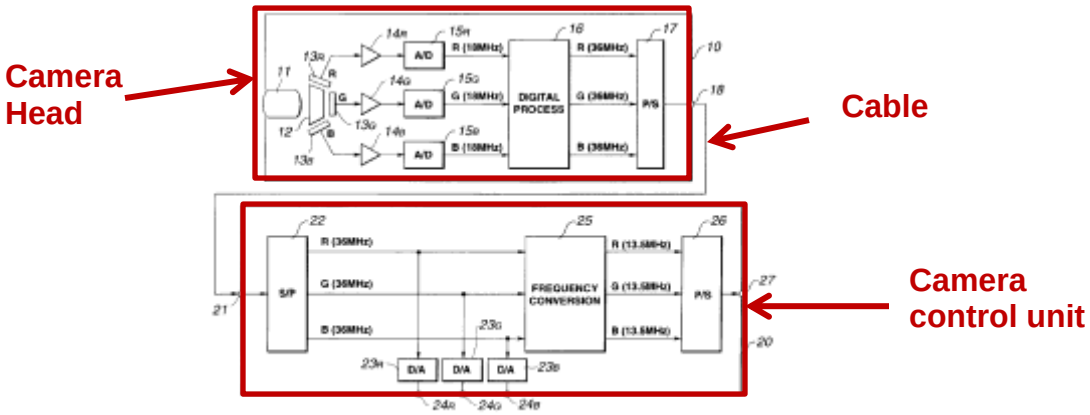


FIG.2

(Ex. 1108, Nakamura at Fig. 2 (annotated); *see also* Nakamura at 1:8-10 ("This invention relates to a method and apparatus for transmitting digital video signals obtained on imaging by a CCD imaging device."), 4:25-26; Ex. 1109, Grindon Decl. at ¶ 109.)

Second, Nakamura discloses a "*camera head*." (*See* Ex. 1109, Grindon Decl. at ¶ 110.) Figure 2 of Nakamura (shown above) illustrates the "camera" connected to the cable. (*See* Ex. 1108, Nakamura at Fig. 2; *id.* at 4:27-46 ("Referring to FIG. 2, the light from an object, incident on a lens system 11 of a camera head 10, is sent to a color-separation prism 12. . . . In the camera head shown in FIG. 2, the CCDs 13R, 13G and 13B are arranged so that the CCDs 13R and 13B for R and B are horizontally offset by one-half the pixel pitch with respect to the CCD 13G for G.") (emphasis added); *id.* at 5:23-30 ("Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 18, compatibility in format is maintained between the camera head 10 and the camera control unit.")

Third, Nakamura discloses that the camera head includes "*an imager generating a stream of video data*." Nakamura states that "[t]he lens system 11 includes . . . a lens for imaging the light from the object on a CCD . . . ." (Ex. 1108, Nakamura at 4:27-39.) (*See also id.* at 4:40-54 ("These R, G and B light beams are converted by the associated CCDs 13R, 13G and 13B into imaging signals associated with R, G and B, respectively.").) Nakamura also states that its apparatus is "for transmitting digital color video signals whereby video signals imaged by a CCD imaging device and outputted will be transmitted to a camera control unit without lowering the resolution for outputting high-resolution video signals." (Ex. 1108, Nakamura at 3:26-32.) The imager of Nakamura generates a stream of video data. (*See also* Ex. 1109, Grindon Decl. at ¶ 111.)

Fourth, Nakamura discloses that the camera head includes "*at least one digital driver*." The "digital driver" of Nakamura is "output terminal 18" in the camera head, which sends the "serial digital video signals . . . via a cable or the like to an input terminal 21 of the camera control unit 20." (Ex. 1108, Nakamura at 5:27-28.) One of ordinary skill in the art would have understood at the time of the alleged invention that transmitting a serial digital cable from an output terminal over a cable necessarily and inherently involves a driver to drive the signal. (*See* Ex. 1109, Grindon Decl. at ¶ 112.)

Fifth and Sixth, "*a processor*" and "*a memory device, accessible by said*

processor, containing camera head information" in the camera head are found in Okada. (*See also* Ex. 1109, Grindon Decl. at ¶ 113.) Okada discloses a "first CPU" on the "scope side" (i.e., camera head). (Ex. 1104, Okada at 4:4-15.) The CPU "controls the total" of the timing circuits and switching. (*Id.*) Okada also discloses a "ROM" memory on the "scope side." (Ex. 1104, Okada at Fig. 1.) Okada discloses that "to the first CPU 20 [on the camera head] a ROM 21 storing setting data . . . is connected." (*Id.* at 4:16-28.) And Okada discloses that "the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit . . ." (*Id.* at 4:58-5:3.)

It would have been obvious in view of Okada to provide a processor on the camera head and a memory on the camera head, to enable the use of different camera heads. (*See* Ex. 1109, Grindon Decl. at ¶ 114.) For example, the combination would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) Specifically, including a processor with access to a memory in the camera head would be advantageous because such a processor and memory would allow for local processing and use of the information in the memory. (*See id.*) One of ordinary skill in the art would have looked to other video imaging systems, including in the field of endoscopes, to conclude that a processor on the camera head would be an obvious way to

implement interchangeable camera heads. (*See id.*) At the time of the alleged invention of the '530 and '530 patents, the advantages of interchangeable camera heads were well-known. (*See id.*) It would have been obvious to employ the processors and memory including information about the camera head in a video imaging system because interchangeability of camera heads would be advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*)

Seventh, Nakamura discloses "*a cable*." (*See* Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20.") (emphasis added). (*See also* Ex. 1109, Grindon Decl. at ¶ 115.)

Eighth, Nakamura discloses "*a camera control unit coupled to said camera head via said cable*." (*See* Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20. The serial digital video signals of R, G and B, supplied to the camera control unit 20, are converted by an S/P conversion circuit 22 into R, G and B component digital video signals.") (emphasis added) (*See also* Ex. 1109, Grindon Decl. at ¶ 116.)

Ninth, Nakamura discloses that the camera control unit has "*at least one digital receiver*." This limitation is again found in Nakamura by virtue of it

disclosing transmitting digital serial information over a cable from a camera to a control unit. (*See above*.) One of ordinary skill in the art at the time of the alleged invention would have known that transmitting a serial digital signal over a cable necessarily and inherently requires a digital serial receiver to receive the digital serial signal that is transmitted. (*See* Ex. 1109, Grindon Decl. at ¶ 117.)

Tenth, Nakamura discloses the "*camera control unit processing a stream of digital video data*." (*See* Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20. The serial digital video signals of R, G and B, supplied to the camera control unit 20, are converted by an S/P conversion circuit 22 into R, G and B component digital video signals.") (emphasis added) (*See also* Ex. 1109, Grindon Decl. at ¶ 118.)

Eleventh, the combination of Nakamura and Okada discloses "*a plurality of camera heads are attachable to and controlled by said camera control unit*." (See Ex. 1109, Grindon Decl. at ¶ 119.) Okada provides for the interchangeability of two different types of cameras, i.e. either a camera designed for the NTSC system or a camera designed for the PAL system. For example, Okada states "it is possible to form and display both the picture data of the NTSC system and the picture data of the PAL system by using the CCD 1 for the NTSC system. Furthermore, in the above example, it is also possible to form and display the pictures of both systems

by the processing similar to that of the above, by using a CCD 1 suitable for the scanning line of the PAL system, and furthermore, it is also possible to use a CCD for the PAL as an imaging element, and the scanning line change circuit in that case is made to perform the compression action." (Ex. 1104, Okada at 6:10-19.)

Again, adding a memory and processor in a camera head would have enabled interchangeable camera heads, which would have been an improvement over a single-camera imaging system. (*See* Ex. 1109, Grindon Decl. at ¶¶ 120-121.) Interchangeable camera heads would be advantageous to allow replacement camera heads in the event of malfunction, or different shaped camera heads for different circumstances. (*See id.*) Providing interchangeable camera heads to the imaging system of Nakamura would have involved merely the use of a known technique to improve a similar system in the same way, and/or the predictable use of prior art elements according to their established functions. (*See id.*)

(ii) Claim 2:

Nakamura discloses that "*said camera head further comprises a timing generator for generating a timing signal particular to said camera head, wherein the timing signal actuates said imager*." Nakamura states that that "[t]he A/D conversion circuits 15R, 15G and 15B digitally convert the analog imaging signals, using the clocks of the same frequency as that of the sampling clocks in the CCDs 13R, 13G and 13B. In the A/D conversion circuit 15G for G, digital conversion is

performed with clocks delayed in phase by 180° from the A/D conversion circuits 15R and 15B for producing the pixel offsetting effect. In the embodiment of FIG. 2, the frequency of the digital imaging signals outputted by the A/D conversion circuits 15R, 15G and 15B is 18 MHz." (Ex. 1108, Nakamura 492 at 4:54-64 (emphasis added).) This is shown below:

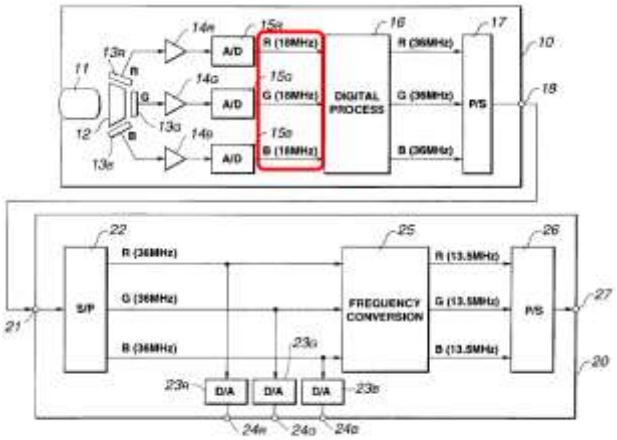


FIG.2

(Ex. 1108, Nakamura at Fig. 2 (annotated).) (*See also id.* at 5:48-61 ("[S]ince the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks, it becomes possible to output video signals of high resolution obtained by pixel offsetting from the camera control unit 20.") The processes that occur in the camera head, such as analog-to-digital conversion, digital signal processing, and frequency conversion, all require timing signals generated by a timing generator. (*See* Ex. 1109, Grindon Decl. at ¶ 122.) A person of ordinary skill in the art would know that the timing for the CCD devices must be derived from a timing source in common with the

clock signals that drive the processes to maintain synchronization. (*See id.*) The timing signal used to actuate the imager is embedded in the serial data signal sent to the CCU. (*See id.*)

Alternatively, this element is disclosed in Okada, which describes "on the scope side" a "timing generator 16." (Ex. 1104, Okada at 4:4-15, Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35.) The timing signal of Okada thus actuates the imager and is sent to the camera control unit. (*See also* Ex. 1109, Grindon Decl. at ¶ 123.)

To the extent not already disclosed in Nakamura, it would have been obvious in view of Okada to provide a timing generator particular to the camera head to actuate the imager. (*See id.* at ¶ 124.) For example, the combination would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) That is because including the timing signal generator in the camera head and sending that timing signal to the camera control unit would have been a simple substitution or improvement, and it would have provided the predictable result of allowing for the interchangeability of camera heads and synchronization of the camera head and camera control unit. (*See id.*)

Allowing the camera head to generate a timing signal that is sent to the camera control unit and used to control the camera control unit would allow the two devices to remain synchronized even if the camera control unit operates with a plurality of different camera heads. (*See id.*)

(iii) Claim 3

Nakamura discloses that "*the timing signal is sent to said camera control unit*." Nakamura describes that the timing signal transmitted from the camera head to the control unit sets the limit resolution of the camera control unit (i.e., "controls" the camera control unit). (*See* Ex. 1108, Nakamura at 5:48-61 ("[T]he limit resolution obtained from the 36 MHz rate digital video signals obtained with the digital processing circuit 206 [sic: inadvertently refers to FIG. 1] of the camera head 200 [sic: inadvertently refers to FIG. 1] is ideally approximately 1400. This rate is maintained when the digital video signals are transmitted to the camera control unit 20. Therefore, the R, G and B component digital video signals outputted at the output terminals 24R, 24G and 24B of the camera control unit 20 are of the above-mentioned resolution. That is, since the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks, it becomes possible to output video signals of high resolution obtained by pixel offsetting from the camera control unit 20.").) (*See also* Ex. 1109, Grindon Decl. at ¶ 125.)

Alternatively, Okada again discloses a "timing generator" and discloses that on the control unit side, "picture data is written in the imaging memory 24A in the timing of the synchronization signal formed in the timing generator 16, and after that, this picture data is read out in the same timing to be stored in the display memory 24B. . . . Then, each of these signals of R, G, and B is outputted to a monitor . . ." (Ex. 1104, Okada at 5:21-35.) Thus, the camera control unit is "controlled" at least in part by the timing signal. (*See* Ex. 1109, Grindon Decl. at ¶¶ 126-127.) Including the timing signal generator in the camera head and sending that timing signal to at least partially control the camera control unit would have been obvious because such a timing signal would allow for the interchangeability of camera heads and synchronization of the camera head and camera control unit. (*See id.*) Doing so would have involved merely the use of a known technique to improve a similar system in the same way and/or the predictable use of prior art elements according to their established functions. (*See id.*) The known method of a camera heading generating a timing signal that is sent to the camera control unit and used to control the camera control unit, would predictably allow the camera head and camera control unit to remain synchronized even if the camera control unit interoperates with a plurality of different camera heads. (*See id.*) Again, interchangeable camera heads would have been an improvement to allow replacement camera heads in the event of malfunction, or different shaped camera

heads for different circumstances. (*See id.*)

(iv) Claim 4

Nakamura that "*said imager produces analog image data and said camera head further comprises a converter for converting the analog image signal to a digital image signal*." Nakamura discloses that "[t]he imaging signals for R, G and B from the CCDs 13R, 13G and 13B are amplified by associated pre-amplifiers 14R, 14G and 14B, respectively, and subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits 15R, 15G and 15B, respectively." (Ex. 1108, Nakamura at 4:50-64 (emphasis added), Fig. 2.) (*See also* Ex. 1109, Grindon Decl. at ¶ 128.)

(v) Claim 5

Nakamura also discloses that "*said camera head further comprises a multiplexer for generating a multiplexed signal, wherein the multiplexed signal includes the image signal and control signals*." The '310 patent states that "[c]ontrol signals include any signal transmitted from the camera head except image data." (Ex. 1101, '310 patent at 4:1-2.). Nakamura states that "[t]he above-mentioned R,G and B component digital video signals, obtained by the digital processing circuit 16, are converted by a P/S conversion circuit 17 into serial composite digital video signals which are outputted along with various other sorts of the information at an output terminal 18." (Ex. 1108, Nakamura 492 at 5:18-26

(emphasis added).) Because the serial composite video signals "are outputted along with various other sorts of the information," the composite video signals necessarily and inherently must be multiplexed. (*See also* Ex. 1109, Grindon Decl. at ¶ 129.) Moreover, the control signals from the sampling clocks of the CCD are necessarily and inherently embedded in the composite video signals. (*See id.*)

(vi) Claim 6

Nakamura discloses that "*said camera head further comprises a serializer for serializing the image signal*." Nakamura discloses that "[t]he above-mentioned R, G and B component digital video signals, obtained by the digital processing circuit 16, are converted by a P/S [parallel to serial] conversion circuit 17 into serial composite digital video signals which are outputted along with various other sorts of the information at the output terminal 18." (Ex. 1108, Nakamura at 5:18-23.) These "serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20." (*Id.* at 5:27-29.) (*See also* Ex. 1109, Grindon Decl. at ¶ 130.)

(vii) Lack of Secondary Considerations

There are no secondary considerations of which Petitioner is aware that would tend to show that the combination of Nakamura and Okada is non-obvious—particularly any having a nexus to the claimed invention. (*See* Ex. 1109, Grindon Decl. at ¶ 131.)

(viii) Claim Charts

The below claim charts contain detailed citation to disclosure in Nakamura and Okada that discloses each element of claims 1-6 of the '530 patent.

'530 Patent Claim 1	**Nakamura in Combination With Okada**
1. A video imaging system comprising:	Ex. 1108, Nakamura at Fig. 2; *see also* Nakamura at 1:8-10 ("This invention relates to a method and apparatus for transmitting digital video signals obtained on imaging by a CCD imaging device."), 4:25-26. Ex. 1104, Okada 852 at 3:58-61 ("FIG. 1 is a block diagram showing the circuit configuration of an electronic endoscope equipped with both the NTSC system and the PAL system according to an embodiment of the present invention."), 1:12-16, Fig. 1.)
a camera head	Ex. 1108, Nakamura '492 at Fig. 2; *id.* at 4:27-46 ("Referring to FIG. 2, the light from an object, incident on a lens system 11 of a camera head 10, is sent to a color-separation prism 12. . . . In the camera head shown in FIG. 2, the CCDs 13R, 13G and 13B are arranged so that the CCDs 13R and 13B for R and B are horizontally offset by one-half the pixel pitch with respect to the CCD 13G for G."); *id.* at 5:23-30, 5:27-33. Ex. 1104, Okada '852 at 4:4-15 ("In FIG. 1 and FIG. 2, the circuit configuration of an electronic endoscope according to the embodiment is shown. In FIG. 1, the CCD 1 arranged on the scope side is an imaging element . . . . Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected.").)
including an imager generating a stream of video data,	Ex. 1108, Nakamura '492 at 4:27-39 ("The lens system 11 includes . . . a lens for imaging the light from the object on a CCD . . . ."), 4:40-54 ("These R, G and B light

	beams are converted by the associated CCDs 13R, 13G and 13B into imaging signals associated with R, G and B, respectively. . . The imaging signals for R, G and B from the CCDs 13R, 13G and 13b . . . are subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits . . .").) Ex. 1104, Okada '851 at 4:4-15, Fig. 1.
at least one digital driver,	Ex. 1108, Nakamura '492 at 5:18-23, 5:27-29 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20.")
a processor,	Ex. 1104, Okada '852 at 4:4-15 ("[A] first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected."), Fig. 1.
and a memory device, accessible by said processor, containing camera head information;	Ex. 1104, Okada 852 at 4:16-28 ("[T]o the first CPU 20, a ROM 21 storing setting data for the control meeting the NTSC system or the PAL system is connected."), Fig. 1, 4:58-5:3 ("the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set"), 4:4-15, Okada at 4:16-28 ("ROM 21 stor[es] setting data for the control meeting the NTSC system or the PAL system [and] is connected . . to the first CPU 20 [on the camera head]."), 4:58-5:3 ("the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit . . .")
a cable; and	Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20.").
a camera control unit coupled to said	Ex. 1108, Nakamura '492 at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal

camera head via said cable	18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20. The serial digital video signals of R, G and B, supplied to the camera control unit 20, are converted by an S/P conversion circuit 22 into R, G and B component digital video signals.") Ex. 1104, Okada '852 at 4:34-40 ("external processor side").
and having at least one digital receiver;	Ex. 1108, Nakamura '492 at 5:27-29 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20.").)
said camera control unit processing a stream of digital video data;	Ex. 1108, Nakamura at Fig. 2 and 5:27-33 ("The serial digital video signals outputted at the output terminal 18 are sent via a cable or the like to an input terminal 21 of the camera control unit 20. The serial digital video signals of R, G and B, supplied to the camera control unit 20, are converted by an S/P conversion circuit 22 into R, G and B component digital video signals.") Ex. 1104, Okada at 4:34-40 ("external processor side").
wherein a plurality of camera heads are attachable to and controlled by said camera control unit.	Ex. 1104, Okada '852 at 4:58-5:3, 5:21-35, Fig. 1, 4:58-5:20, 6:10-19 ("Thus, in this example, it is possible to form and display both the picture data of the NTSC system and the picture data of the PAL system by using the CCD 1 for the NTSC system. Furthermore, in the above example, it is also possible to form and display the pictures of both systems by the processing similar to that of the above, by using a CCD 1 suitable for the scanning line of the PAL system, and furthermore, it is also possible to use a CCD for the PAL as an imaging element, and the scanning line change circuit in that case is made to perform the compression action.").
'530 Patent, Claim 2	**Nakamura in Combination With Okada**
2. The video imaging system according to	Ex. 1108, Nakamura 492 at 4:54-64 ("The A/D conversion circuits 15R, 15G and 15B digitally convert

claim 1 wherein said camera head further comprises a timing generator for generating a timing signal particular to said camera head, wherein the timing signal actuates said imager.	the analog imaging signals, using the clocks of the same frequency as that of the sampling clocks in the CCDs 13R, 13G and 13B. In the A/D conversion circuit 15G for G, digital conversion is performed with clocks delayed in phase by 180° from the A/D conversion circuits 15R and 15B for producing the pixel offsetting effect. In the embodiment of FIG. 2, the frequency of the digital imaging signals outputted by the A/D conversion circuits 15R, 15G and 15B is 18 MHz."), Fig. 2, 5:48-61 ("[S]ince the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks, it becomes possible to output video signals of high resolution obtained by pixel offsetting from the camera control unit 20."), 5:18-30. Ex. 1104, Okada '852 at 4:4-15 ("In FIG. 1, the CCD 1 arranged on the scope side is an imaging element for the NTSC system having a number of scanning lines or the like suitable for the scanning line of the NTSC system, and to this CCD 1, a timing generator 16 is connected, and to this timing generator 16, an NTSC crystal oscillator 17, a PAL crystal oscillator 18, and a switching device 19 are provided. Furthermore, a first CPU 20 is provided, which controls the total while controlling this switching device 19, and by the control of this first CPU 20, either of the oscillators 17, 18 is selected."), Fig. 1, 5:4-20 ("That is, if the NTSC system is selected, the NTSC system oscillator 17 is connected to the timing generator 16 by the switching circuit 19. . . . the driving pulse based on this is given to the CCD 1."); *id.* at 5:21-35, 5:48-56.
'530 Patent, Claim 3	**Nakamura in Combination With Okada**
3. The video imaging system according to claim 2 wherein the timing signal is sent to said camera control unit.	Ex. 1108, Nakamura '492 at 5:48-61 ("[T]he limit resolution obtained from the 36 MHz rate digital video signals obtained with the digital processing circuit 206 of the camera head 200 is ideally approximately 1400. This rate is maintained when the digital video signals are transmitted to the camera control unit 20. Therefore, the

	R, G and B component digital video signals outputted at the output terminals 24R, 24G and 24B of the camera control unit 20 are of the above-mentioned resolution. That is, since the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks, it becomes possible to output video signals of high resolution obtained by pixel offsetting from the camera control unit 20.").) Ex. 1104, Okada '852 at 4:58-5:3 ("[T]his second CPU 26 reads out the setting data of the selected system from the ROM 27 to set the processing contents of each circuit by this setting data. At the same time, the information of the selected system is also transmitted to the first CPU 20 on the scope side from this second CPU 26, and on this scope side, the selected setting data is read out from the ROM 21 by the first CPU 20 to set the processing contents of each circuit, and further, either of the above oscillators 17, 18 is selected and set."), 5:21-35, Fig. 1, 4:58-5:20.
'530 Patent, Claim 4	**Nakamura in Combination With Okada**
4. The video imaging system according to claim 1 wherein said imager produces analog image data and said camera head further comprises a converter for converting the analog image signal to a digital image signal.	Ex. 1108, Nakamura '492 at 4:50-64 ("The imaging signals for R, G and B from the CCDs 13R, 13G and 13B are amplified by associated pre-amplifiers 14R, 14G and 14B, respectively, and subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits 15R, 15G and 15B, respectively."), Fig. 2. Ex. 1104, Okada '852 at 4:29-33 ("[T]o the CCD 1, an AGC (automatic gain control) circuit including a CDS (correlative double sampling) circuit is connected similarly to that in the prior art, and to this AGC circuit 5, a DSP (digital signal processor) circuit 22 is connected through an A/D converter 6.")
'530 Patent, Claim 5	**Nakamura in Combination With Okada**
5. The video imaging system according to	Ex. 1108, Nakamura 492 at 5:18-26 ("The above-mentioned R,G and B component digital video signals,

claim 1 wherein said camera head further comprises a multiplexer for generating a multiplexed signal, wherein the multiplexed signal includes the image signal and control signals.	obtained by the digital processing circuit 16, are converted by a P/S conversion circuit 17 into serial composite digital video signals which are outputted along with various other sorts of the information at an output terminal 18.")
'530 Patent, Claim 6	**Nakamura in Combination With Okada**
6. The video imaging system according to claim 1 wherein said camera head further comprises a serializer for serializing the image signal.	Ex. 1108, Nakamura '492 at 5:18-23 ("The above-mentioned R, G and B component digital video signals, obtained by the digital processing circuit 16, are converted by a P/S [parallel to serial] conversion circuit 17 into serial composite digital video signals which are outputted along with various other sorts of the information at the output terminal 18."), 5:27-29.

F. Ground 6: Claims 8-9 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura, Okada (Processor and Memory Reference) and Adler (LVDS Reference)

As discussed above in Section V.D., Nakamura in combination with Okada would have rendered obvious all of the features of independent claim 1. In addition, it would have been further obvious in view of Adler to use LVDS in such a video system. Using LVDS communication protocol in the combination of Nakamura and Okada would have satisfied all of the limitations of claims 8-9.

Again, Adler teaches a video imaging system for an endoscope, comprising a camera head, camera control unit, and cable. (Ex. 1105, Adler at Fig. 1; *see also*

id. at 9:24-38; Ex. 1109, Grindon Decl. at ¶ 134.) The camera control unit of Adler processes a continuous stream of digital video data from the camera head, through the cable. (*See, e.g.*, Ex. 1105, Adler at 9:24-33 ("The configuration comprises a miniature endoscopic front-end 10, hereinafter simply referred to as an endoscope, attached by a wire connection 20 to a processing device 30, typically a PC, the PC having appropriate software for carrying out image processing of the output of the endoscope.") (emphasis added); *see also id.* at 9:39-47, 5:21-23 ("Preferably, the dedicated image processor is a motion video processor . . . .")

Adler, however, specifically discloses LVDS data transmission. Adler states that "[t]he electrical signals are digitized and passed to a transmitting device 62, for example an LVDS transmitter, which drives the data through communication link 20 and adapter 44 to the processing device 30." (Ex. 1105, Adler 940 at 10:7-19 (emphasis added).) (*See also* Ex. 1109, Grindon Decl. at ¶ 135.) One of ordinary skill in the art would have recognized that LVDS is an alternative communications protocol that is particularly appropriate for video applications because it has a high bit rate. (*See* Ex. 1109, Grindon Decl. at ¶ 135.) One of skill in the art would understand a higher bit rate is more advantageous in video applications because it can transfer data more quickly. (*See id.*)

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention of the '530 patent to add the LVDS

communication protocol of Adler to the combination of Nakamura and Okada. (*See* Ex. 1109, Grindon Decl. at ¶¶ 137-139.) Specifically, one of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system). (*See id.* at ¶ 136.) The combination would have involved the known method of simply replacing Nakamura/Okada's digital serial drivers and receivers with comparable LVDS modules, as disclosed in Adler. (*See id.* at ¶ 137.) The result would have been predictable; that is, the resulting system would merely use the LVDS protocol and LVDS drivers and receivers to transmit information between the camera head and camera control unit. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. (*See* Ex. 1109, Grindon Decl. at ¶ 138.) LVDS was an improved communication protocol because it was particularly appropriate for video applications. (*See id*.) LVDS would have been attractive due particularly to its higher data rates, lower power, and adaptability to lower voltages, which is more advantageous in video applications because it can transfer data more quickly. (*See id*.) LVDS would have improved Nakamura/Okada by providing the same benefits as the TI-LVDS reference. (*See id*.)

There are no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 140.)

G. Ground 7: Claims 8-9 Are Obvious Under 35 U.S.C. §103(a) in View of Nakamura, Okada (Processor and Memory Reference) and TI-LVDS (LVDS Reference)

As discussed above in Ground 6, it would have been obvious at the time of the alleged invention of the '530 patent to substitute LVDS as the digital serial communication protocol in the combination of Nakamura and Okada, as well as utilize bi-directional drivers and receivers. In Ground 6, Petitioner relied on Adler for disclosure of LVDS and bi-directional drivers and receivers in a camera system very similar to those of Nakamura and Okada. Adler, however, is again prior art under 35 U.S.C. §102(e). Should the Board determine that Patent Owner KSEA is able to swear behind Adler as prior art, the TI-LVDS reference is again an example of §102(b) prior art that discloses LVDS in a digital video system. Accordingly, Ground 7 is non-redundant to Ground 6, because Ground 7 relies on §102(b) prior art for LVDS instead of §102(e) prior art.

As previously discussed, Exhibit 1006 (the TI-LVDS reference) is cited on the face of the '530 patent as prior art non-patent literature. (*See* Ex. 1101, '530 patent at 2.) TI-LVDS discloses the use of LVDS digital serial drivers and digital serial receivers (i.e., the use of digital serial drivers and receivers on both the

camera head and camera control unit). (*See* Ex. 1106, TI-LVDS at Fig. 1 (showing drivers and receivers on both the camera head and camera control unit); Ex. 1109, Grindon Decl. at ¶¶ 143-145.) In fact, the '530 patent references digital serial drivers and digital serial receivers manufactured by Texas Instruments that implement the LVDS standard. (*See, e.g.*, Ex. 1101, '530 patent at 6:56-61.) Figure 1 of TI-LVDS shows "a typical connection with LVDS drivers and receivers." (Ex. 1106, TI-LVDS at 6-7.) Thus, the use of LVDS for transmitting digital data was well-known prior to the alleged '530 patent invention. (*See* Ex. 1109, Grindon Decl. at ¶¶ 143-145.)

For the identical reasons discussed above in Ground 6 with respect to Nakamura, Okada, and Adler, it would have been obvious to utilize the LVDS communication protocol in TI-LVDS in the combination of Nakamura and Okada. (*See id.* at ¶¶ 146-147.) Specifically, one of skill in the art would have understood that LVDS was a desirable alternative for communicating image and control signals between a camera head and camera control unit in a digital video imaging system). (*See id.* at ¶¶ 146-147.) The combination would have involved the known method of simply replacing Nakamura/Okada's digital serial drivers and receivers with comparable LVDS modules. (*See id.* at ¶ 146.) The result would have been predictable; that is, the resulting video imaging system would merely use LVDS serial communication protocol and LVDS drivers and receivers to

transmit information between the camera head and camera control unit. (*See id.*)

Alternatively, the combination would have been obvious because it results from the use of a known technique to improve a similar system in the same way, or from the application of a known technique to a known system that is ready for improvement, to yield predictable results. LVDS was an improved communication protocol because it was particularly appropriate for video applications, with higher data rates, lower power, and adaptability to lower voltages. (*See id.*) It would have been obvious to employ the high bit rate of the LVDS in Nakamura/Okada because a higher bit rate is more advantageous in video applications because it can transfer data more quickly. (*See id.*) LVDS would have improved the combination in the same way as the TI-LVDS reference. (*See id.*)

There are no secondary considerations of which Petitioner is aware that would tend to show that this combination is non-obvious—particularly any having a nexus to the claimed invention. (*See id.* at ¶ 148.)

VI. REASONS WHY PROPOSED GROUNDS ARE NON-REDUNDANT

Petitioner respectfully submits that each of the above-proposed grounds is non-redundant. Eto and Nakamura are both primary references that disclose video imaging systems having most of the elements of the ‘530 patent claims. Eto and Nakamura, however, disclose the various ‘530 patent claim elements (such as the camera head, control unit, cable, serializer, digital driver, digital receiver, and

analog-to-digital converter) in different ways.

Okada discloses the same type of video imaging system, but specifically for use in an endoscope. Okada also discloses interchangeable camera heads through the use of a processor and memory on the camera head. Adler and TI-LVDS are the only references disclosing LVDS communication protocol. Adler, however, is §102(e) prior art, while TI-LVDS is §102(b) prior art. King discloses more detailed disclosure of a timing signal generator, and controlling the camera control unit in response to a timing signal.

Further, each of the grounds in this petition is non-redundant with a second petition filed on the same day by Petitioner asserting invalidity of claims 1-6, 8-9 of the '530 patent. That petition raises an anticipation ground (whereas this petition raises only obviousness grounds), and it raises alternative obviousness grounds based on different primary references that are non-redundant.

VII. CONCLUSION

For the above reasons, Petitioner respectfully requests institution of *inter partes* review of claims 1-6, 8-9 of the '530 patent.

Dated: February 19, 2015

Respectfully submitted,

/s/ Robert A. Surrette

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CERTIFICATE OF SERVICE

I hereby certify that true and correct copies of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,821,530 and Exhibits 1101-1111 were served on February 19, 2015 via pre-paid, overnight Federal Express to the correspondence address for the attorneys of record for Karl Storz Endoscopy USA, the assignee of U.S. Patent No. 7,821,530:

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