Paper No. 1
Filed: July 18, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NEVRO CORP.,
Petitioner,

v.

BOSTON SCIENTIFIC NEUROMODULATION CORP.,
Patent Owner.

Case No. IPR2019-01315
U.S. Patent No. 7,127,298

Petition for Inter Partes Review of
U.S. Patent No. 7,127,298

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I. INTRODUCTION

Petitioner Nevro Corp. ("Nevro"/"Petitioner") requests *inter partes* review (IPR) of claims 1-19 ("challenged claims") of U.S. Patent No. 7,127,298 ("'298 patent"). The '298 patent is directed to a particular configuration of a multi-channel implantable stimulator, a medical device that uses electrodes to stimulate nerves in, for example, a patient's ear or spine.

According to the '298 patent, in prior art multi-channel stimulators, each channel had its own current source connected to its own electrode. The '298 patent explains that while multi-channel stimulators are beneficial, the one-to-one ratio between current sources and electrodes disadvantageously required more space within the stimulator. The '298 patent, therefore, seeks to reduce stimulator size by requiring fewer current sources while maintaining the ability to stimulate electrodes on multiple channels with different parameters. The '298 purports to enable this reduced size by using a number of switches that are a function of the number of current sources and electrodes. The Examiner allowed the claims based on the understanding that they required "a multi-channel stimulator specifically limiting the number of switching elements to be determined from the number of electrode contacts/groups multiplied by the number of digital-to-analog converters present," and that the claimed combinations were not disclosed by the prior art before the Examiner. Ex. 1002, 22.

The state of the art for multi-channel implantable stimulators was well-developed by the '298 patent's claimed October 2002 priority date. Multi-channel cochlear, spinal, and cardiac stimulators were already being used with patients. At that time there was already "a constant need and desire to make such implantable devices smaller and smaller." Ex. 1012, 1:63-65. And it was known that one way to do that was to have a switching matrix selectively connect electrode pairs to current sources, "rather than designing a separate current source for each electrode pair." *Id.*, 2:4-16. Beyond that known concept, the claims are merely a routine implementation of switches that connect a smaller number of current sources to a larger number of electrodes. Each configuration of current sources, switches, and electrodes set forth in the challenged claims is disclosed in the prior art.

For the reasons set forth below, the prior art references relied upon herein anticipate or render obvious each of the challenged claims. The challenged claims are unpatentable and should be cancelled.

II. COMPLIANCE WITH IPR REQUIREMENTS

A. Certification of Standing (37 C.F.R. § 42.104(a))

Nevro certifies that the '298 patent is available for IPR and Nevro is not barred or estopped from requesting an IPR of the challenged claims on the grounds identified below. Neither Nevro nor any of its privies has filed a civil action challenging the validity of any claim of the '298 patent. This petition is timely

filed within one year of the service of BSNC's complaint alleging infringement of the '298 patent on July 19, 2018. *See* Ex. 1010.

B. Mandatory Notices (37 C.F.R. § 42.8)

1. Real Party-in-Interest

Nevro Corp. is the real party-in-interest for this petition.

2. Related Proceedings

The '298 patent claims priority to U.S. Provisional Patent Application No. 60/419,684.

The '298 patent is at issue in the following case: *Boston Scientific Corp. et al. v. Nevro Corp.*, Case No. 1-18-cv-00644 (D. Del.).

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Nevro consents to service via electronic mail at its counsels' addresses above.

C. Fees

The Director is authorized to charge any fees due during this proceeding to Deposit Account No. 50-1597.

D. Service on Patent Owner

Pursuant to 37 C.F.R. § 42.105(a) and the Certificate of Service, the petition and exhibits have been served on the correspondence of record for the '298 patent.

III. IDENTIFICATION OF CHALLENGED CLAIMS

Claims 1-19 of the '298 patent are unpatentable under 35 U.S.C. §§ 102-103 as follows:

Ground 1. Claims 1-5 and 11-14 are anticipated by Hitzelberger (Ex. 1005).

Ground 2. Claims 1-5 and 11-14 are obvious over Hitzelberger (Ex. 1005).

Ground 3. Claims 2-3 and 12-13 are obvious over Hitzelberger (Ex. 1005) in view of Panescu (Ex. 1008).

Ground 4. Claims 1-5 and 11-14 are obvious over Panescu (Ex. 1008) in view of Faltys (Ex. 1009).

Ground 5. Claims 6-10 and 15-19 are anticipated by Jones (Ex. 1006).

Ground 6. Claims 6-10 and 15-19 are obvious over Jones (Ex. 1006).

Ground 7. Claims 7-8 and 16-17 are obvious over Jones (Ex. 1006) in view of Panescu (Ex. 1008).

As further explained below, each prior art reference relied upon by Nevro is prior art to the '298 patent, which claims priority to a provisional application filed

on October 18, 2002.[1] Nevro's challenges are further supported by the declaration and testimony of Mr. Ben Pless (Ex. 1003), an expert in implantable medical devices with over 30 years of experience. *See* Ex. 1003, ¶¶2-8, 50; Ex. 1004 (CV).

Nevro's patentability challenges do not advance "the same or substantially the same prior art or arguments previously … presented to the Office." *See* 35 U.S.C. § 325(d). The prior art relied on by the present petition was not previously considered by the Examiner during prosecution of the '298 patent. The Examiner also did not have the benefit of the detailed testimony of Mr. Pless and the further evidence of record.

IV. THE '298 PATENT

A. Overview

The '298 patent is directed to an implantable stimulator, such as a "cochlear device for restoration of hearing" or a "spinal cord stimulation [("SCS") device] for treating intractable pain." Ex. 1001, 1:12-27. The '298 patent specifically claims a multi-channel device. *Id.*, claims 1-19, *see also* Ex. 1001, Face ("Switched-Matrix Output for Multi-Channel Implantable Stimulator"); Ex. 1003, ¶30.

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[1] For purposes of this Petition, Nevro has assumed that the '298 patent's priority date is October 18, 2002. *See* § IV.C below.

The ’298 patent explains that “multi-channel, implantable stimulators presently have the capability of driving up to 16 electrodes and have increased processing capability.” Ex. 1001, 1:28-30. Digital to analog converters (DACs) drive the electrodes and, according to the ’298 patent, “occupy a high percentage of the space used by the analog circuitry…” *Id.*, 3:53-55, 4:6-15. The ’298 patent describes alternative embodiments that uses switching schemes to allow electrode contacts to share DACs. *Id.*, 4:6-10, 4:15-21; Ex. 1003, ¶31. This can “reduce the overall size of the implanted device” or allow the use of “a larger battery in the saved space to enable more channels, more processing power or longer device life.” *Id.*, 1:49-55.

1. Figure 3 Embodiment: Claims 1-5 and 11-14

Figure 3 shows one embodiment of the ’298 patent where N number of DACs (11, shown in blue) are connected to M electrode contacts (31, shown in green) using N x M total number of switches (21, shown in yellow). Ex. 1001, 4:22-34; Ex. 1003, ¶32. This is illustrated in Figure 3:

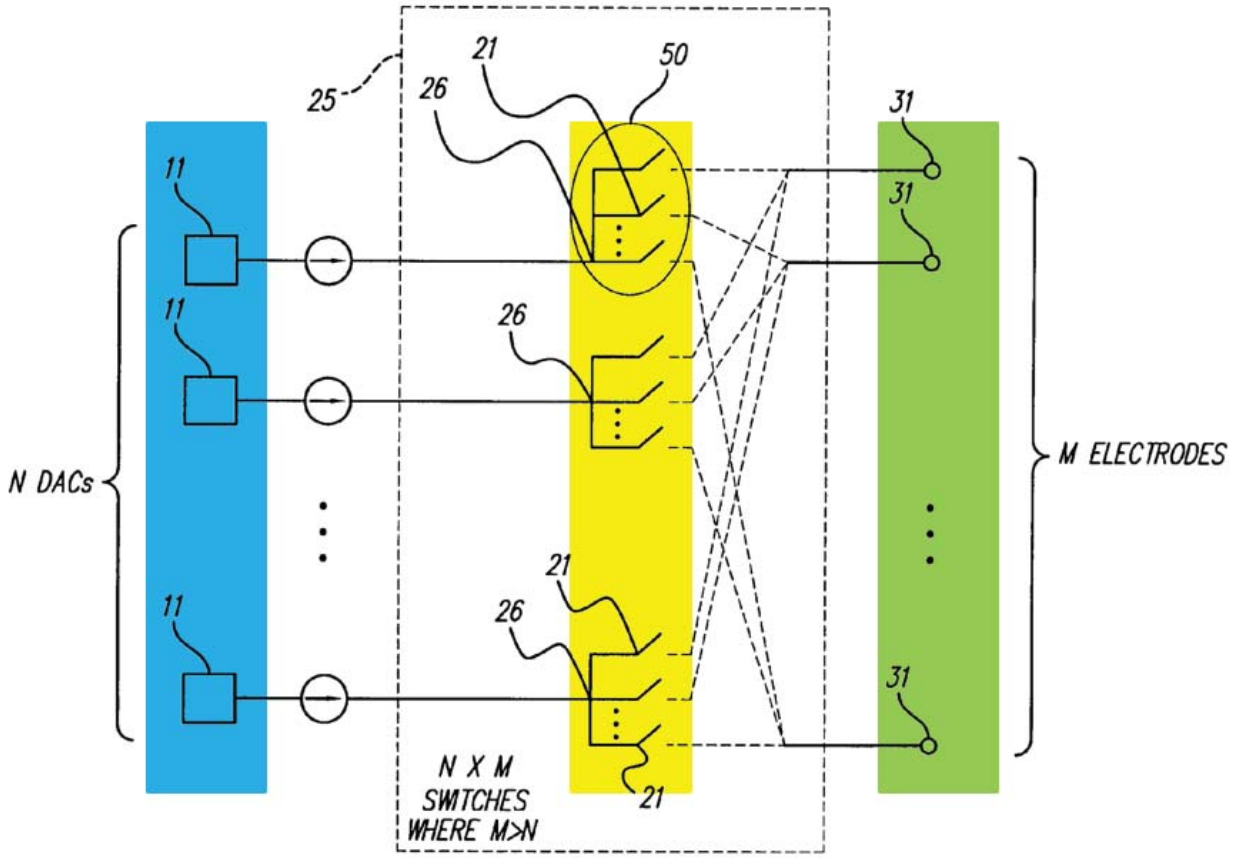


FIG. 3

Ex. 1001, Fig. 3 (annotated); Ex. 1003, ¶32.

In the Figure 3 embodiment, each DAC (11) has its own set of M switches (50) that allow it to connect to any of the M electrodes (31). Ex. 1001, 4:27-31. DACs 11 can operate simultaneously and the switches (21) select which electrodes are stimulated. *Id.*, 4:58-62; Ex. 1003, ¶33. Claims 1-5 and 11-14 relate to the Figure 3 embodiment.

2. Figure 4A Embodiment: Claim 6-10 and 15-19

Figure 4A is an additional embodiment of the '298 patent. Unlike the Figure 3 embodiment, the Figure 4A embodiment does not connect every DAC (12) to every electrode (130). Ex. 1001, 5:8-22; Ex. 1003, ¶36. Instead, each DAC (12) is connected to a single electrode (130) in each electrode group or set (100). Ex. 1003, ¶¶35-36. This embodiment "takes advantage of the fact that, in many multi-channel stimulators, not all stimulation channels are active (turned on) at a given moment." Ex. 1001, 5:10-13. The Figure 4A embodiment includes N number of DACs (12, shown in blue) that are each connected to their own sets of L switches (110), for a total of M switches (121, shown in yellow), *i.e.*, N x L = M. *Id.*, Fig. 4A.

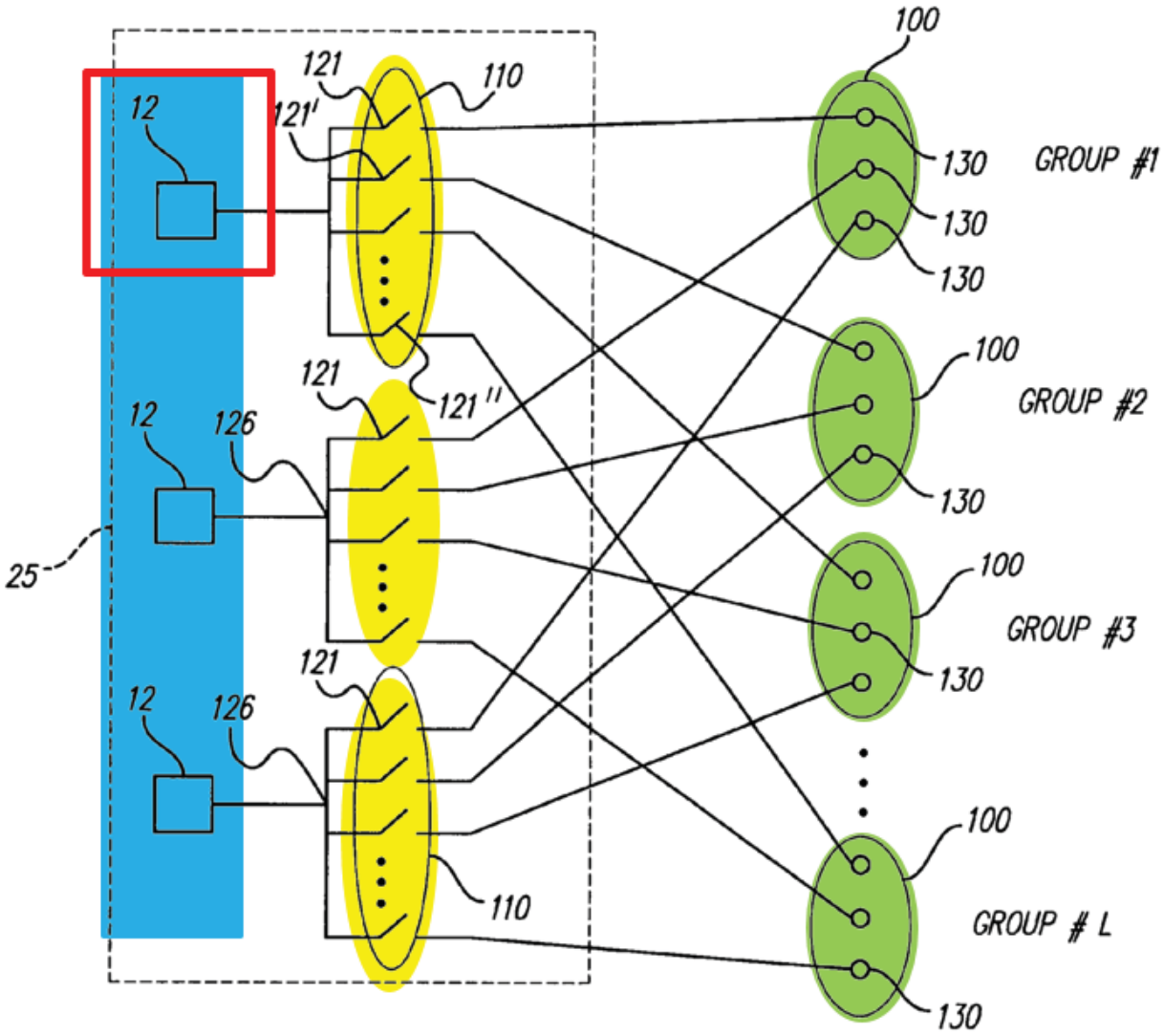


FIG. 4A

Ex. 1001, Fig. 4A (annotated), 5:8-21; Ex. 1003, ¶35.

Each set of L switches includes a single connection to each of L groups or sets of electrodes (100, shown in green), labeled #1 through #L. Ex. 1003, ¶35. For example, and as shown above, the top DAC (shown in the red square) is connected to the top electrode in each electrode group (highlighted in the green)

via a switching set (110, highlighted in yellow). Ex. 1003, Fig. 4A; Ex. 1003, ¶35. Claims 6-10 and 15-19 relate to the Figure 4A embodiment.

B. Background on Multi-Channel Implantable Stimulators

The state of the art for multi-channel implantable stimulators was well developed by October 18, 2002, the earliest claimed priority date of the '298 patent. Ex. 1003, ¶39. The '298 patent identifies cochlear devices and SCS systems as exemplary multi-channel implantable stimulators. Ex. 1001, 1:15-27. By the late 1990s, the prior art already recognized that there has been "continual need to provide very low power sensors" and "a constant need and desire to make such implantable devices smaller and smaller." Ex. 1012, 1:63-65; Ex. 1003, ¶40. "To meet this need (smaller circuits, less power) within an implantable stimulating device, it has been common to design an output circuit for interfacing with the electrodes which ***selectively connects*** a single current source***, or one of a plurality of current sources, to a selected electrode pair, rather than designing a separate current source for each electrode pair***." Ex. 1012, 1:66-2-5 (emphasis added); Ex. 1003, ¶40.

It was also well-recognized by the late 1990s that such "one DAC per electrode" systems take up too much space. *E.g.*, Ex. 1006, 1211 ("[T]he area taken up by the DAC's (and their associated circuitry) is such that it may not be practical to employ one DAC per electrode on the chip."). Ex. 1003, ¶41. As the

prior art recognized, however, "this many DAC's would not be required" because "it is possible to time-demultiplex the pulses coming from a DAC, and use one DAC to stimulate a number of electrode sites." Ex. 1006, 1211; Ex. 1003, ¶41.

C. Effective Filing Date and Prosecution History

The '298 patent was filed as Application No. 10/686,219 on October 15, 2003, and claims priority to Provisional Application No. 60/419,684, filed on October 18, 2002. Ex. 1001, Face. Each of the prior art references in this petition was filed or published well before October 18, 2002, so whether the '298 patent is entitled to its earliest claimed priority date of October 18, 2002, is not relevant to Nevro's patentability challenge. Nevro's analysis assumes an October 18, 2002 priority date. *See* Ex. 1003, ¶42.

The Examiner allowed claims 1-19 of the '298 patent without any rejections, and provided the following "statement of reasons for allowance":

> Independent claims 1, 6, 11, and 15 recite a multi-channel stimulator specifically ***limiting the number of switching elements to be determined from the number of electrode contacts/groups multiplied by the number of digital-to-analog converters present***. The prior art discloses multi-channel stimulators containing the elements above, however, fail to describe alone or in combination the specific limitation of the claimed invention. Therefore, the Examiner deems independent claims 1, 6, 11, and 15 and their depending claims allowable over the prior art.

Ex. 1002, 22 (emphasis added); Ex. 1003, ¶43.

D. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '298 patent in 2002 would have had (1) at least a bachelor's degree in electrical engineering, biomedical engineering, or equivalent coursework, and (2) at least one year of experience researching or developing implantable medical devices. Ex. 1003, ¶48; *see also id.*, ¶¶44-50.

V. CLAIM CONSTRUCTION

Claims in an IPR are given their "ordinary and customary meaning … as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b); 83 Fed. Reg. 51,358 (Oct. 11, 2018). Nevro is unaware of any "prior claim construction determination" related to the '298 patent. *See* 37 C.F.R. § 42.100(b).

A. "Multi-Channel Stimulator" (All Claims)

Each claim recites a "*multi-channel stimulator*." In the context of the claims of the '298 patent, a "*multi-channel*" stimulator must be interpreted to require more than one DAC to be capable of simultaneously providing stimulation to two or more channels with different stimulation parameters. Ex. 1003, ¶51.

As an initial matter, the "multi-channel stimulator" as used in the preambles to the challenged claims should be interpreted as limiting because it "is necessary

to give life, meaning, and vitality to the claim." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999) (Finding preamble limiting because "it is essential that the court charged with claim construction construe the preamble and the remainder of the claim, as we have done here, as one unified and internally consistent recitation of the claimed invention.") (internal citation omitted). "Multi-channel stimulator" is necessary to understand the claimed invention because it unifies the limitations in the bodies of the claims and explains how the elements operate together. Ex. 1003, ¶52; *see, e.g., Optimum Processing Solutions, L.L.C. v. Advanced Micro Devices, L.L.C.*, C.A. No. 1:09-CV-1097-TCB, 2012 WL 13001396, at *6 (N.D. GA July 10, 2012) (finding "computer" in preamble is limiting where expert testified that it "breathes life into the claims" and is needed "in order to understand the claims").

The specification repeatedly emphasizes that the present invention relates to a multi-channel stimulator. *See, e.g.*, Ex. 1001, Title (Switched-Matrix Output for ***Multi-Channel*** Implantable ***Stimulator***), 1:12-14 (The present invention relates to implantable stimulators and, specifically, ***methods and systems for delivering stimulation through multiple output channels***); 1:32-34 ("The ***long-term trend is toward using more channels*** while more processing capability is added.) (emphasis added). That it is a "stimulator" explains how the electrodes powered by DACs via a switching system operate when in use. Ex. 1003, ¶53.

Additionally, "multi-channel" explains the functional interplay between the claim limitations requirements that there be multiple DACs with a higher number of electrode contacts than DACs in order to achieve the space-saving goals of the patent while still providing the "multi-channel" capabilities that are emphasized in the intrinsic evidence. Ex. 1003, ¶53; *see also Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1375 (Fed. Cir. 2008) (finding that "portable computer" in the preamble is a limitation because this feature was emphasized in the intrinsic evidence).

That the claims require that the stimulator have more than one DAC is consistent with the stated goal of the '298 patent. Ex. 1003, ¶54. The '298 patent explains that, in the prior art, "[f]or a sixteen channel monopolar stimulation system, sixteen DACs would need to be used with the conventional output method." Ex. 1001, 3:66-4:1. While the trend was to "increase the total number of stimulation channels in order to gain increased stimulation flexibility," "increasing the number of stimulation channels will undesirably increase the number of DACs and, disadvantageously, require the use of additional space in the medical device." *Id.*, 4:5-10. Accordingly, the '298 patent's stated goal is to "provide a switching system and method which permits use of fewer DACs then electrode contacts, thereby saving limited device space" while also maintaining the advantages of being able to stimulate on multiple channels. Ex. 1001, 2:47-50 *see also id.*, 4:18-

21 ("The present invention … enables more stimulation channels (and electrode contacts) to be added while reducing the use of spacing consuming DACs.").

The claims and specification make clear that the '298 patent is directed to a "multi-channel stimulator" that can provide multiple channels with fewer DACs than channels, but more than one DAC is still required for the system to be multi-channel. Ex. 1003, ¶55.

Each of the '298 patent claims themselves require more than one DAC. Ex. 1003, ¶56. For example, claim 1 states that "***each*** DAC (11) of the N number of ***DACs*** is coupled uniquely to one group (50) of M number of switches (21)" (emphasis added). As an initial matter, the claim's use of "each" with reference to the "N number of ***DACs***," indicates a plurality. Moreover, the claim requires that the DACs are "coupled uniquely" to one group of switches, further demonstrating that the stimulator has more than one DAC. The other independent claims contain comparable language. Ex. 1001, claim 6 ("wherein each DAC of the N number of DACs…"); claim 11 ("coupling each of N DACs…"); claim 15 ("coupling each of N DACs…").

Similarly, the specification describes only multi-channel stimulators, which have more than one DAC. Ex. 1003, ¶57. In addition, the specification explains that having multiple DACs or current sources provides the multi-channel stimulator with the capability to stimulate on multiple channels at the same time

with different stimulation parameters: "Each of the N number of DACs ***may*** provide a current that is ***a different or same amplitude***. Not all the DACs need to be operating at the same time. It is also ***possible that the DACs are all operating at the same time***, but the switches, which may be programmed, can be closed to permit current to flow through only selected electrode contacts 31." Ex. 1001, 4:57-63 (emphasis added); s*ee also id.*, 5:2-7 ("Thus, while there are only N number of DACs, which is less than M, the number of electrode contacts, ***it may be possible to activate every electrode contact 31 at one time,*** although some of the electrode contacts may have the same level of current flowing as they derive from the same DAC."); 5:65-6:3 (same).

VI. CLAIMS 1-19 ARE UNPATENTABLE

A. Claims 1-5 and 11-14 Are Anticipated by Hitzelberger (Ex. 1005)

1. Overview of Hitzelberger

Hitzelberger et al., *A Microcontroller Embedded ASIC for an Implantable Electro-Neural Stimulator*, Proceedings of the 27th European Solid-State Circuits Conference (ESSCIRC), 428-431 (Frontier Group 2001) ("Hitzelberger") is a paper that was published and publicly disseminated as part of the 2001 ESSCIRC conference in Villach, Austria. Ex. 1015, ¶¶11-18. Dr.-Ing. Yiannos Manoli, a co-author of the Hitzelberger paper, has been extensively involved in ESSCIRC conferences since the late 1980s. Ex. 1015, ¶¶6-8. He explains that ESSCIRC

conferences are open to the public and attended by members of industry and academia who are interested in microelectronics. *Id.*, ¶9. ESSCIRC conferences are advertised on its website, via calls for papers, and via a program distributed to its mailing list that identifies papers to be presented and distributed at the conference. *Id.*; *e.g.*, Ex. 1018, 1-3, 34.

Every ESSCIRC participant receives hardbound and electronic copies of the papers published at the conference. Ex. 1015, ¶9. Dr. Manoli attended the 2001 conference and received, along with every other participant, hardbound (Ex. 1019) and electronic (Ex. 1005) copies of the Hitzelberger paper. Ex. 1015, ¶¶13-14, 18; Ex. 1016 (CD index of papers); Ex. 1017 (CD documentation). The Hitzelberger paper also was later distributed to libraries. *E.g.*, Ex. 1020 (Mar. 2002 date-stamp). Hitzelberger was therefore published and disseminated to the public by late 2001, and is prior art under 35 U.S.C. § 102(b) (pre-AIA).

Hitzelberger discloses that "implantable micro-electronic systems" can be used for "the electrical stimulation of nerves which have lost their natural functionality" such as "restoring basic movement abilities of a disabled hand, caused by a spinal cord injury." Ex. 1005, p. 1. Hitzelberger's system uses "two current-output digital-to-analog converters" to generate "two independently controlled currents on one or more of 12 neural electrodes." *Id.* Figure 1 illustrates the overall system, including two DACs:

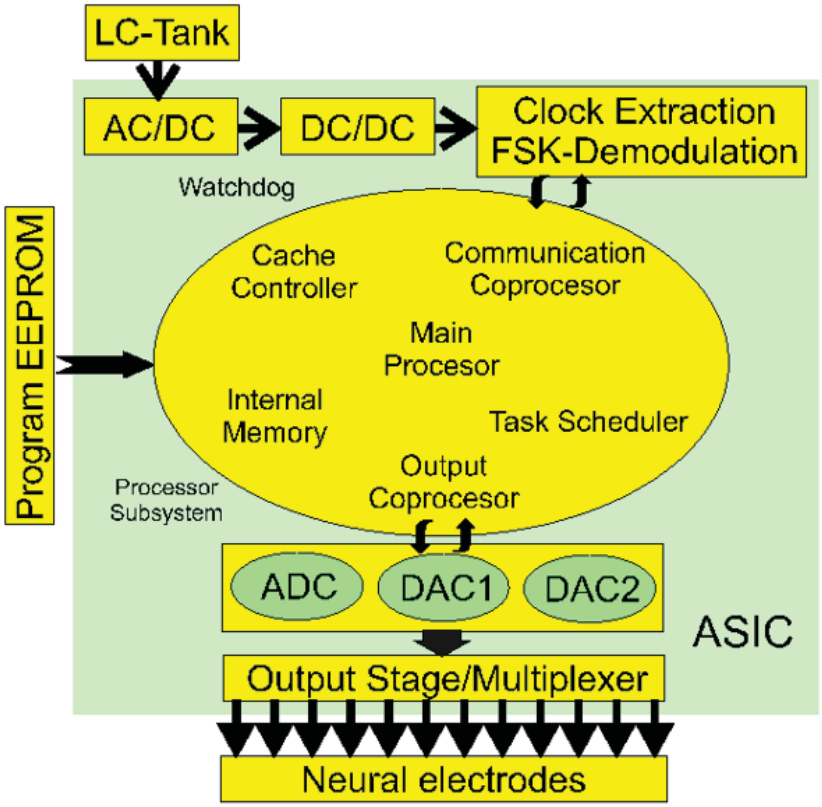


Figure 1. System Block Diagram

Ex. 1005, p. 1; Ex. 1003, ¶68.

The "multi-tasking processor subsystem" includes a "second coprocessor" which "starts feeding the DACs with data and controlling the multiplexers" after "activation through the task scheduler." Ex. 1005, 3. Two DACs connect to a "multiplexing output stage" such that "[u]p to 12 neural electrodes can be stimulated and time multiplexed." *Id.* Figure 5 illustrates how the DACs interact with the multiplexers and electrodes:

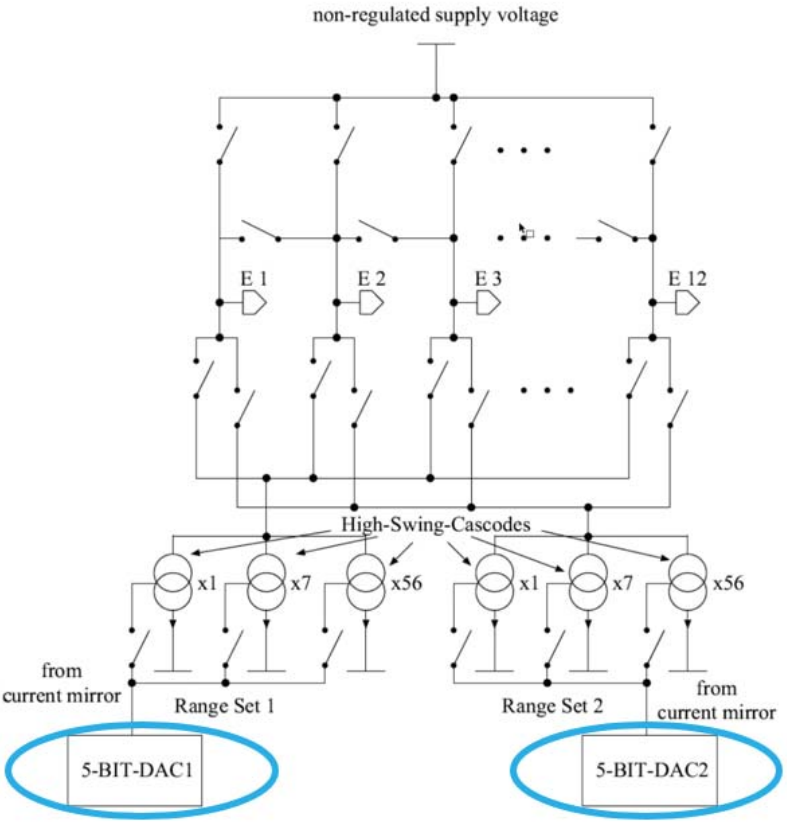


Figure 5. Multiplexing Output Stage

Ex. 1003, 3, Fig. 5 (annotated), Ex. 1003, ¶69.

The "output stage contains a switching matrix (see Figure 5) which allows [it] to individually connect each electrode to each of the two current sinks or to V_{DD} as well as to other electrodes." Ex. 1005, 3. This "enables simple bipolar neural stimulation … as well as more sophisticated schemes." *Id*. Important stimulation variables include "not only amplitude, frequency and stimulation waveform, but also the current density distribution." *Id.*

Because there are two DACs and 12 electrodes, Hitzelberger specifies that two channels can be stimulated simultaneously at different stimulation parameters:

Table 1. Technical Summary

Die Size:	42 mm^2
# Transistors:	220.000
Clock Frequency:	0.25 - 4 MHz
Communication:	
Carrier Frequency:	4 (3-5) MHz
Modulation, Δf:	$+/-37.5kHz$
FSK Uplink, Manch.coded:	80 kBit/s
LSK Downlink, Manch.coded:	4.8 kBit/s
Stimulation:	
No. of Channels	12, 2 simult.
Current Range:	1 μA - 2 mA
Current Resolution:	min. 1 μA
Waveform Resolution:	min. 1 μs
Power:	
Supply Voltage:	3.3 (6) V
Input Current:	2.7mA
On chip rectifier and regulator:	
AC-Input Amplitude:	4.2 V to 9 V
DropVoltage:	100 mV min.
Efficiency:	~ 85%

Ex. 1003, 4, Table 1 (annotated); Ex. 1003, ¶71.

2. Claim 1

i. *Preamble*

Claim 1 recites "*[a] stimulation output switching system for a multi-channel stimulator, said system comprising: ….*" Hitzelberger discloses this limitation. Ex. 1003, ¶¶72-75.

Hitzelberger discloses an application specific integrated circuit (ASIC) that is a component in an "implantable, batteryless electro-neural stimulation system." Ex. 1005 (Hitzelberger), 1 (Abstract); *see also id.*, 4 same quote). The system

"allows for [the] stimulation of nerves with two independently controlled currents on one or more of 12 neural electrodes." Ex. 1005, 1. The implant includes, *inter alia*, "two current-output digital-to-analog converters" (DACs), a "multiplexing input/output stage," and the neural electrodes, shown in Figures 1 and 5 below:

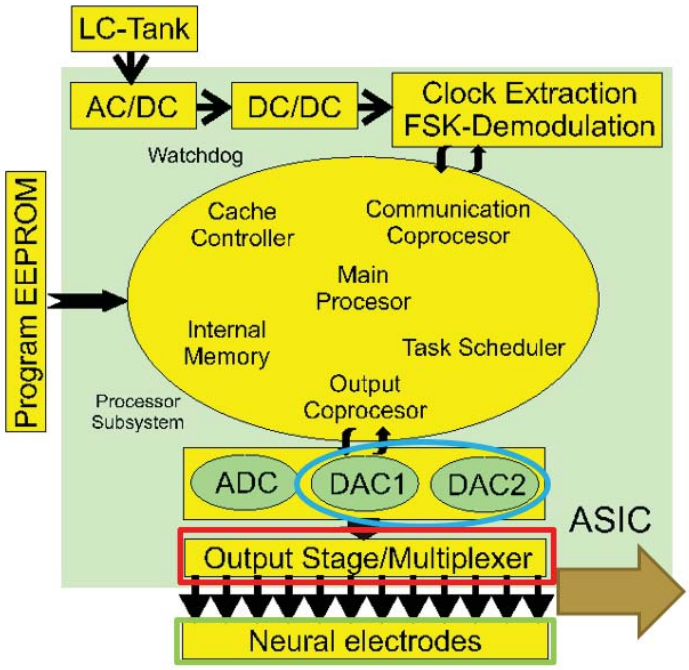


Figure 1. System Block Diagram

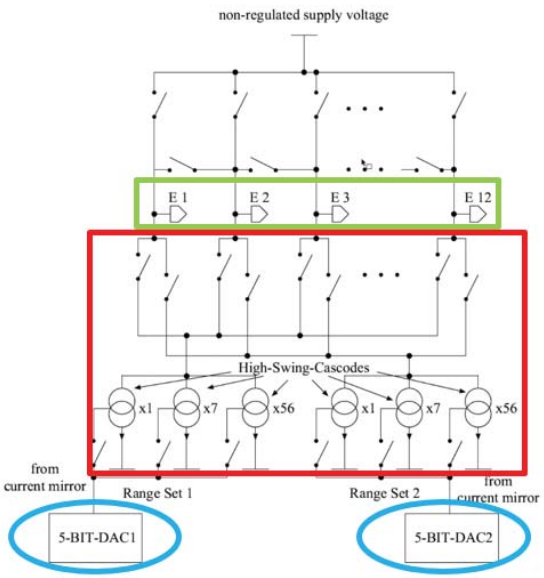


Figure 5. Multiplexing Output Stage

Ex. 1005, Figs. 1 and 5 (annotated), p1, 3; Ex. 1003, ¶73. The "output stage contains a switching matrix (see Figure 5) which allows [it] to individually connect to each electrode" (electrodes shown in green above; output stage/multiplexer shown in red above). Ex. 1005, 3; Ex. 1003, ¶73.

As explained by Mr. Pless, Hitzelberger's system is a "*multi-channel stimulator*" because it is capable of using its two DACs to stimulate two different

electrodes simultaneously with different stimulation parameters (e.g., current amplitude). Ex. 1003, ¶74. Hitzelberger expressly discloses the capability of stimulating on two channels simultaneously. Ex. 1005, 4 ("**Stimulation**: No. of Channels 12, 2 simult.") (emphasis in original); Ex. 1003, ¶74. In addition, Hitzelberger discloses that DACs can work together to stimulate electrodes simultaneously: "[t]herefore, when using a multipolar cuff electrodes for stimulation [2], the second DAC can work as a steering current." Ex. 1005, 4. A POSA would have understood this disclosure to mean that one DAC provides some of the current for stimulation, while the other DAC simultaneously provides a variable amount of additional current that steers the site of stimulation. Ex. 1003, ¶75; *see also id.*, 4 ("It allows simultaneous stimulation of up to 12 neural electrodes and is controlled and powered using an RF transcutaneous telemetry link."). A POSA would have further recognized that this means both DACs would be activated simultaneously and at different stimulation parameters. Ex. 1003, ¶75. Based on these teachings, and as explained by Mr. Pless, Hitzelberger discloses a "*multi-channel stimulator*." Ex. 1003, ¶75.

ii. *N DACs*

Claim 1 also recites *"N number of DACs (11)."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶76-78. Hitzelberger's system has two "current-output digital to analog converters" (DACs), shown below:

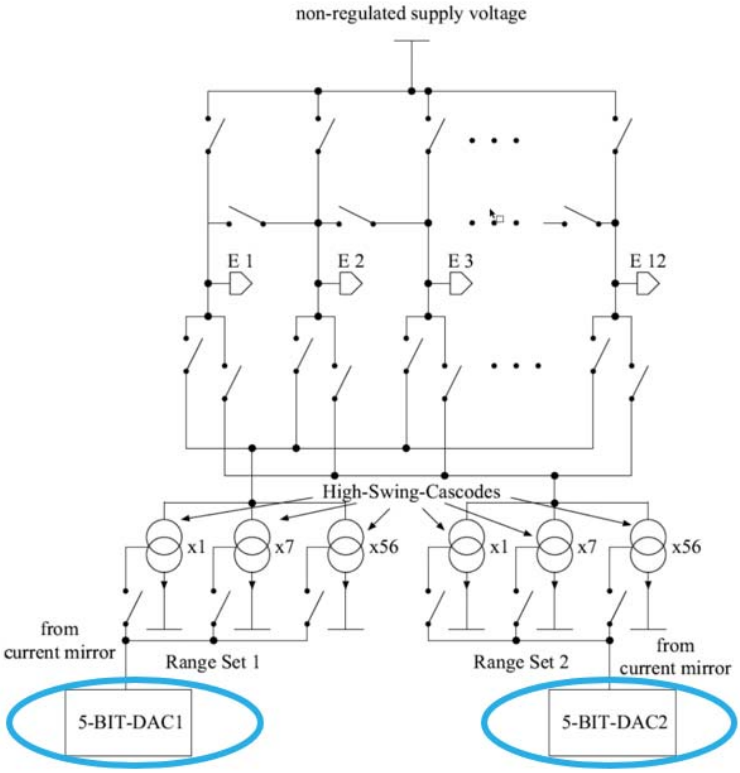


Figure 5. Multiplexing Output Stage

Ex. 1005, Fig. 5 (annotated), 3; Ex. 1003, ¶77.

As shown above, Hitzelberger's system has two "*DACs*," *i.e.*, "5-BIT-DAC1" and "5-BIT-DAC2." Ex. 1005, Fig. 5. Alternatively, Hitzelberger discloses that each DAC is associated with a high-swing cascode amplification circuit that provides for three different current ranges. Ex. 1005, 3. A POSA would have considered the switches of range set 1 and range set 2 to be part of DAC1 and DAC2, respectively. Each combination of DAC and amplification circuit can likewise be considered a "*DAC*" in the context of the claim. Ex. 1003, ¶78. Hitzelberger thus discloses "*N number of DACs*," where N = 2. *Id.*

iii. *M Electrode Contacts*

Claim 1 also recites *"M number of electrode contacts (31) …."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶ 79-81. Hitzelberger discloses 12 neural electrodes, as shown below:

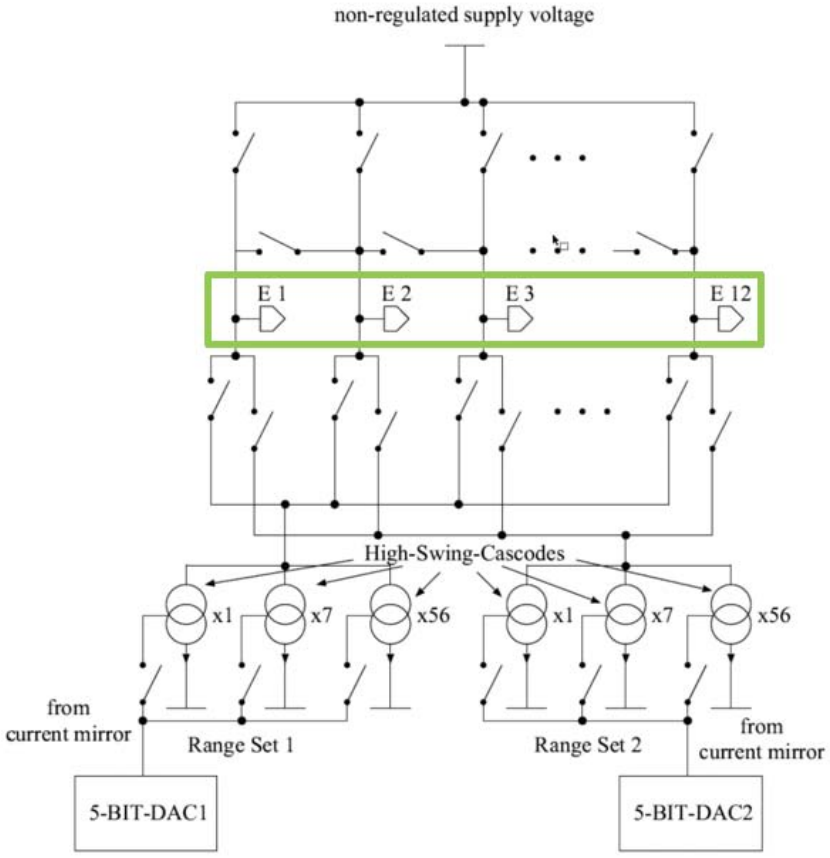


Figure 5. Multiplexing Output Stage

Ex. 1005, Fig. 5 (annotated), 1 ("It allows stimulation on one or more of 12 neural electrodes."); Ex. 1003, ¶80; *see also id.*, p.1 (abstract).

As shown above, Hitzelberger discloses a system with 12 electrodes. Ex. 1005, 3 ("Up to 12 neural electrodes can be stimulated time multiplexed"); Ex.

1003, ¶81; *see also id.*, 4 ("It allows simultaneous stimulation of up to 12 neural electrodes and is controlled and powered using an RF transcutaneous telemetry link."). Hence, Hitlzelberger discloses "*M number of electrode contacts*," where M = 12.

iv. *NxM Switches*

Claim 1 additionally recites *"NxM number of switches (21)."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶82-87. As explained above, Hitzelberger's system has 2 ("N") DACs and 12 ("M") electrodes. Accordingly, N x M = 24 and Hitzleberger discloses 24 switches. For example, Hitzelberger's system has switch pairs (yellow boxes) that connect the electrodes (green boxes) to each DAC source, shown below:

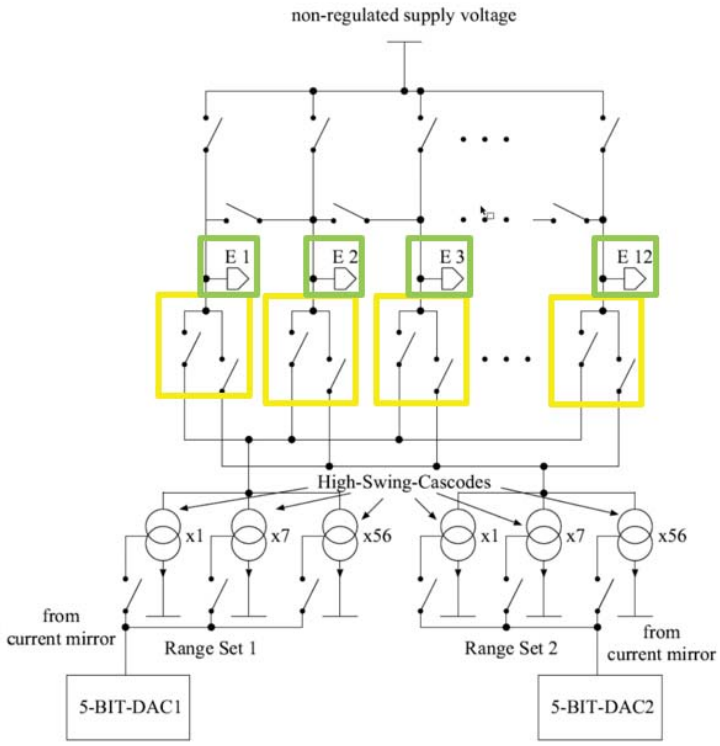


Figure 5. Multiplexing Output Stage

Ex. 1005, Fig. 5 (annotated), 3 ("The output stage contains a switching matrix (see Figure 5) which allows to individually connect each electrode to each of the two current sinks…."); Ex. 1003, ¶84.

A skilled artisan would have understood that there are 24 switches ("*NxM number of switches*") located in the yellow boxes in annotated Figure 5 above. Ex. 1003, ¶85. As explained above, *see* §§VI.A.2.ii and VI.A.2.iii, Hitzelberger discloses 2 DACs and 12 electrodes (green boxes). Accordingly, N = 2 and M = 12 so "*NxM*" is 24. Ex. 1003, ¶85. As shown in the yellow boxes in annotated Figure 5 above, each electrode (*i.e.*, E1 through E12) (green boxes) is connected to

a pair (2) of switches (yellow boxes), so there are 24 (2 x 12) switches. Ex. 1003, ¶85.

The switches associated with the "High-Swing Cascodes" are used to modify the current ranges for each of the DACs and are not relevant to the switching arrangement of the claims, the limitations of which are separately disclosed by the switches emphasized with yellow boxes that control whether the DACs stimulate the corresponding electrodes. *Id.*, 3; Ex. 1003, ¶86. To the extent that Patent owner argues that the range set switches would be included in the "*NxM number of switches*," a POSA would have instead considered the switches of range set 1 and range set 2 to be part of DAC1 and DAC2, respectively. Ex. 1003, ¶86. Accordingly, the switches in range sets above would not have been considered to be switches in "*NxM number of switches*."

Hitzelberger therefore discloses "*NxM number of switches*" by disclosing 24 switches as shown above.

v. *DAC to Switch Coupling*

Claim 1 also recites "*wherein each DAC (11) of the N number of DACs is coupled uniquely to one group (50) of M number of switches (21).*" Hitzelberger discloses this limitation. Ex. 1003, ¶¶88-92. For example, Figure 5 of Hitzelberger shows that each switch is connected to a single DAC, shown below:

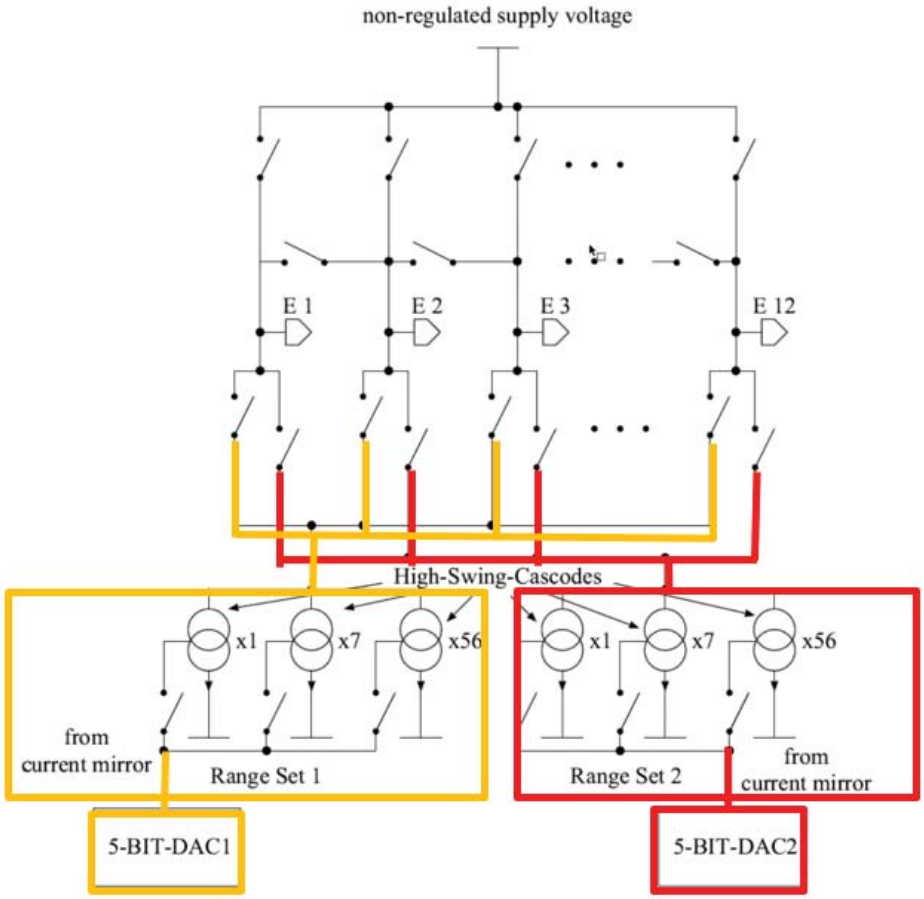


Figure 5. Multiplexing Output Stage

Ex. 1005, Fig. 5 (annotated), 3 ("The analog part consists of 2 current-output digital to analog converters, a multiplexing output stage…. The output stage contains a switching matrix (see Figure 5) which allows to individually connect each electrode to each of the two current sinks…."); Ex. 1003, ¶89.

As shown above, Figure 5 shows two different circuitry groups: an orange circuitry group and a red circuitry group. Ex. 1003, ¶90. In each circuitry group, Hitzelberger's DAC produces a current output. Ex. 1005, 3 ("To minimize the voltage drop, the current of the actual DAC (unity current sources and switches)

are mirrored into the output stage."). As Hitzelberger explains, the "high swing cascodes" multiply the current ranges provided by one of the "current-output digital to analog converters." *Id.* ("Three different current ranges are provided for each converter with multiplication factors of x1, x8, [and] x64 leading to a minimum resolution of 1µA with a maximum output range up to 2mA (Fig. 5.)."); *see also id.* ("The resulting current is finally mirrored by high-swing cascodes and thereby multiplied corresponding to the chosen current range."); Ex. 1003, ¶90. Once multiplied, the result is sent to the switching matrix used to select the appropriate electrodes. Ex. 1005, 3 ("The output stage contains a switching matrix (see Figure 5) which allows to individually connect each electrode to each of the two current sinks…"); Ex. 1003, ¶90.

Accordingly, Hitzelberger discloses that one DAC (*i.e.*, the DAC in the red circuitry group) is connected to one switch group (*i.e.*, the switches in the red circuity group). Ex. 1003, ¶91. Likewise, Hitzelberger discloses that the other DAC (*i.e.*, the DAC in the orange circuitry group) is connected to a different switch group (*i.e.*, the switches in the orange circuitry group). Ex. 1003, ¶91. Hitzelberger therefore discloses two switch groups that are each connected to one of the two DACs.

vi. *Switch to Electrode Contact Coupling*

Claim 1 additionally recites *"each switch within each group (50) of M switches, in turn, is coupled to each one of M electrode contacts (31)."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶93-95. As shown above, *see* § VI.A.2.v, Figure 5 of Hitzelberger shows two switch groups that each have a switch coupled to one electrode. Ex. 1003, ¶94. For example, in the annotated figure below, switch 23 and switch 24 are connected to electrode E12 and belong to the orange and red circuitry groups, respectively, as shown below:

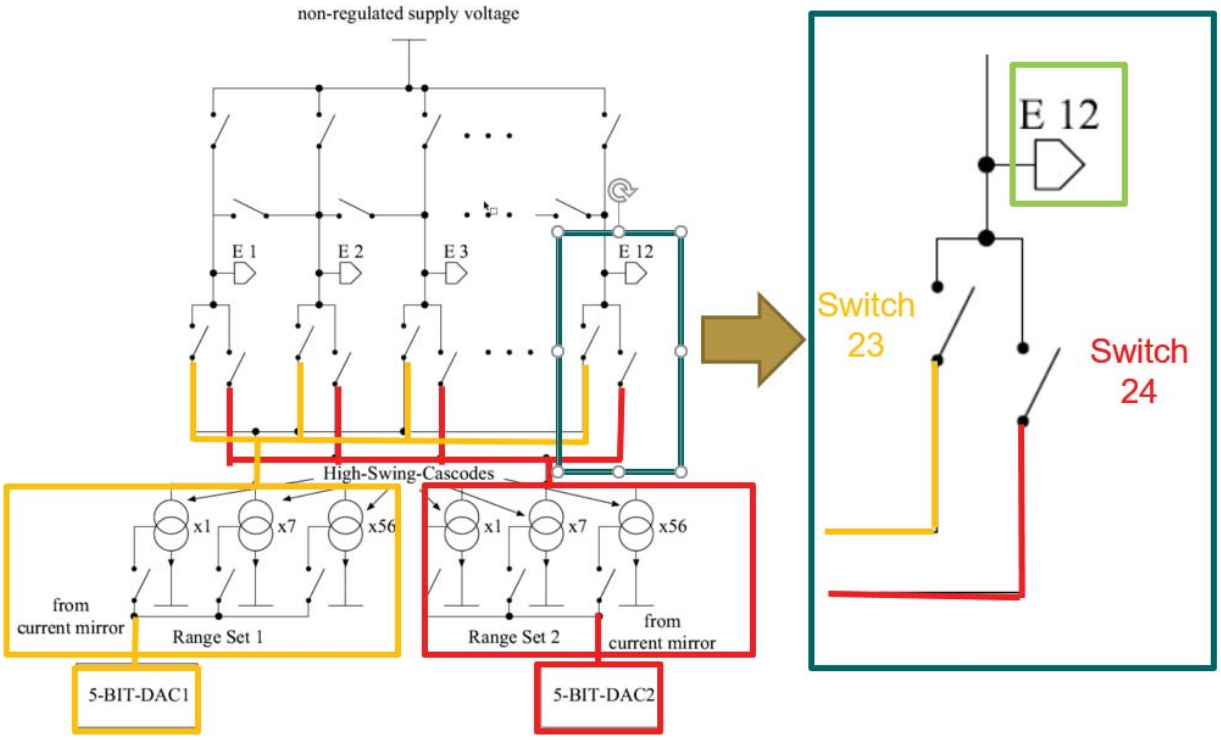


Figure 5. Multiplexing Output Stage

Ex. 1005, Fig. 5 (annotated); *id.*, 3 ("The output stage contains a switching matrix (see Figure 5) which allows to individually connect each electrode to each of the two current sinks…."); Ex. 1003, ¶94. As shown above, Figure 5 of Hitzelberger shows that both the orange and red circuitry groups have switches (*e.g.*, switches 23 and 24 above) coupled to each electrode (*i.e.*, electrodes E1 through E12). Ex. 1003, ¶95.

vii. *Wherein Clause*

Claim 1 also recites *"wherein M and N are whole numbers and M is greater than N."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶ 96-98. As explained above, *see* §§ VI.E.2.ii and VI.E.2.iii, Hitzelberger discloses 2 DACs and 12 electrode contacts. Accordingly, N = 2 ("*N number of DAC*s") and M = 12 ("*M number of electrode contacts*"), both are whole numbers, and 12 is greater than 2. Ex. 1003, ¶97.

3. Claims 2 and 3

Claim 2 recites *"[t]he system of claim 1 wherein the switches are transistor switches,"* and claim 3 recites *"[t]he system of claim 2 wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors."* Hitzelberger discloses these limitations. Ex. 1003, ¶¶99-103.

Hitzelberger discloses that the switches use a "CMOS process." Ex. 1005, 3; Ex. 1003, ¶100. A CMOS transmission gate is "essentially an electronic switch

that is controlled by an input logic level." Ex. 1007, 427. Further, a CMOS transmission gate "consists of one *n*-channel and one *p*-channel MOS transistors connected in parallel." *Id*. Accordingly, Hitzelberger's switches are CMOS switches (*i.e.*, CMOS transmission gates) made up of *n*-channel (NMOS) and *p*-channel MOS (PMOS) transistors. Ex. 1003, ¶¶100, 103.

4. Claim 4

Claim 4 recites *"[t]he system of claim 1 wherein the switches are programmable using software or hardware programming."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶104-106.

Hitzelberger discloses that "[t]he program memory of the main processor is off-chip and is in-circuit ***programmable*** using the communication protocol." Ex. 1005, 1. In particular, Hitzelberger discloses that the "system is controlled and powered using [a]…RF-telemetry link." *Id.* (emphasis added). Hitzelberger discloses that the RF communication can specify "[t]he desired stimulation waveform…by amplitude-period value pairs or a predefined function can be selected from memory and parameterized." Ex. 1005, 2. Once data is received, the task scheduler feeds data to the processor to control the DACs and multiplexer (*i.e.*, switches in multiplexing output stage). Ex. 1003, ¶105; *see also* Ex. 1005, 3 ("After activation through the task scheduler this processor starts feeding the DACs with data and controlling the multiplexers."). Accordingly, Hitzelberger's

chip and its corresponding switches are software programmed from RF-communications provided by the user. Ex. 1003, ¶105.

5. Claim 5

Claim 5 recites "*[t]he system of claim 4, wherein the programming allows one and only one Switch (21), at any one time, to be electrically closed (connected) to one particular electrode contact (31), and thereby permit current to flow through that single electrode contact."* Hitzelberger discloses this limitation. Ex. 1003, ¶¶107-111.

Hitzelberger discloses that the task scheduler feeds the DACs with data and controlling the multiplexers so "[u]p to 12 neural electrodes can be stimulated time multiplexed." Ex. 1005, 3. It explicitly discloses that the system may permit current to flow to a single electrode contact at a time: "It allows stimulation of nerves with two independently controlled currents on ***one*** or more of 12 neural electrodes." *Id.*, 1 (emphasis added). Moreover, Hitzelberger discloses that the two DACs in the ASIC support only two electrode channels of the twelve channels simultaneously. Ex. 1003, ¶108; Ex. 1005, 4 ("No. of Channels: 12, 2 simult."). Accordingly, one of Hitzelberger's DACs supports only a single electrode that is selected by the switching matrix. Ex. 1003, ¶108. Once an electrode is selected, only one of the twelve DAC switches—*i.e.*, the switch associated with the selected electrode—is closed when that electrode is stimulated ("*allows one and only one*

switch… to be electrically closed (connected) to one particular electrode contact and thereby permit current to flow through that single electrode contact"). Ex. 1005, 3 ("Up to 12 neural electrodes can be stimulated time multiplexed."); Ex. 1003, ¶108.

A POSA would have understood that both of Hitzelberger's DACs cannot stimulate the same electrode at the same time. Ex. 1003, ¶109. Although both DACs can operate simultaneously, each DAC must be connected to different electrodes. Ex. 1003, ¶109. For example, Hitzelberger's second DAC may provide current to a different electrode while the first DAC is active. Ex. 1005, 4 ("Therefore, when using a multipolar cuff electrodes for stimulation (2], the second DAC can work as a steering current."). In doing so, the other DAC uses its own switch group to select an electrode thereby allowing simultaneous stimulation of channels. Ex. 1005, 4 ("No. of Channels: 12, 2 simult."); Ex. 1003, ¶110. Once that second electrode is selected, only one of the second DAC's twelve switches—*i.e.*, the switch associated with the second selected electrode—is closed when that second electrode is stimulated. Ex. 1003, ¶110.

The programming described for claim 4 can therefore, *at any one time*, operate the switches to "individually connect" ("*electrically closed (connected)*") one DAC to a selected electrode in order to stimulate the selected electrode

("*permit current to flow through that single electrode contact*"). Ex. 1005, 1; Ex. 1003, ¶111.

6. Claim 11

Claim 11 is disclosed by Hitzelberger for the same reasons described above for claim 1. Specifically, Hitzelberger discloses *"[a] method of switching outputs in a multi-channel stimulator, said method comprising:"* (§ VI.A.2.i) *"(a) providing N number of DACs (11)"* (§ VI.A.2.ii), *"(b) providing M number of electrode contacts (31)"* (§ VI.A.2.iii) *"(c) coupling each of N DACs (11) to a group of M switches (31)"* (§§ VI.A.2.iv-v) *"(d) coupling each of the M switches (31) uniquely to each of M electrode contacts (31)"* (§ VI.A.2.vi), and "*wherein M and N are whole numbers and M is greater than N"* (§ VI.A.2.vii). Ex. 1003, ¶¶112-116, 119.

Hitzelberger further discloses *"(e) connecting selected Switches (21) by closing the Switches, to electrically connect selected electrode contacts (31) to transmit current, while avoiding closing more than one Switch (21) connected to the same electrode contact (31) at any one time, wherein there is at least NxM total number of switches (31).*" Hitzelberger discloses this limitation for the same reasons provided for claim 5. Ex. 1003, ¶117. As explained above (§ VI.A.5), Hitzelberger discloses that each DAC has a several switches associated with individual electrode and, when selected, that switch is closed thereby causing

current to stimulate the electrode ("*closing the switches to electrically connect selected electrode contacts (31) to transmit current*"). Ex. 1003, ¶118; *see* Ex. 1005, ("Up to 12 neural electrodes can be stimulated time multiplexed."). Both DACs can simultaneously provide current to different electrodes as selected by a switch in a DAC's circuitry group (e.g., red or orange circuitry group shown in §VI.A.2.v) ("*connecting selected Switches (21) by closing the switches*") as explained above. *See* §VI.A.5; Ex. 1005, 4 ("No. of Channels: 12, 2 simult."); Ex. 1003, ¶118. As also explained above, *see* §VI.A.5, both of Hitzelberger's DACs cannot stimulate the same electrode contact at any one time, which means that each DAC must necessarily have closed switches associated with different electrodes ("*avoiding closing more than one Switch (21) connected to the same electrode contact (31) at any one time*"). Ex. 1003, ¶118.

7. Claims 12 and 13

Claim 12 recites *"[t]he method of claim 11 wherein the switches are transistor Switches*," and claim 13 recites *"[t]he method of claim 12 wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors."* Hitzelberger discloses this limitation for the same reasons provided for claims 2 and 3. Ex. 1003, ¶120.

8. Claim 14

Claim 14 recites *"[t]he method of claim 11 wherein the step (e) of connecting [s]witches is accomplished by using software or hardware programming."* Hitzelberger discloses this limitation for the same reasons provided for claim 4. Ex. 1003, ¶122.

B. Claims 1-5 and 11-14 Are Obvious Over Hitzelberger

Claims 1 and 11 require "*NxM number of switches*." As discussed above, *see* §§ VI.A.2.ii and VI.A.2.iii, Hitzelberger discloses 2 DACs ("N") and 12 ("M") electrodes, and 24 switches that connects the DACs to the electrodes as required by the claims. Ex. 1005, Fig. 5 (annotated above). To the extent that Patent Owner argues that Hitzelberger does not disclose "*NxM number of switches*" because there are additional switches used in the "range set[s]" above, it would have been obvious to a POSA to modify Hitzelberger to eliminate those switches. Ex. 1003, ¶¶123- 126.

The switches associated with the range sets above are used to modify the current ranges for each of the DACs. *Id.*, 3 ("The resulting current is finally mirrored by high-swing cascodes and thereby multiplied corresponding to the chosen current range."). As explained by Mr. Pless, those additional switches are not relevant to electrode selection, which is handled by the 24 switches emphasized

with yellow boxes that control whether the DACs stimulate the corresponding electrodes. Ex. 1003, ¶125.[2]

Accordingly, it would have been obvious to a POSA to modify the disclosed system to eliminate the switches in the range sets because they provide only additional functionality (*i.e.*, modification of current range). Ex. 1003, ¶126. Where this added functionality is not needed, a POSA would have been motivated to eliminate the switches in a range set because, in a system that does not require modification of the current range, it would simplify the design and conserve resources, saving time and money in design and manufacture. *Id.*

C. Claims 2-3 and 12-13 Are Obvious Over Hitzelberger (Ex. 1006) in view of Panescu (Ex. 1008)

Claims 2 and 12 recite "*wherein the switches are transistor switches.*" Claims 3 and 13 depend on claims 2 and 12, respectively, and further recite "*wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors*." To the extent that Patent owner argues that the Hitzelberger's switches are not "*transistor switches*" that are "*selected from a*

[2] As explained above (§ VI.A.2.ii), a POSA would have considered the switches of range set 1 and range set 2 to be part of DAC1 and DAC2, respectively.

group consisting of PMOS or MOS transistors," such a distinction would have been obvious. Ex. 1003, ¶¶128-133.

MOS and PMOS transistors were a well-known electrical components used for electrical switches. Ex. 1007, 430; Ex. 1003, ¶131. MOS transistors, including PMOS transistors, are "electronic switches that either conduct or are open." Ex. 1007, 430. PMOS transistors were a well-known electrical components used for electrical switches. Ex. 1003, ¶131. For example, U.S. Patent No. 6,101,410 to Panescu et al. ("Panescu") (issued on August 8, 2000; prior art under 35 U.S.C. § 102(b) (pre-AIA)) discloses an ASIC with switches made up of PMOS transistors. Ex. 1008, 10:50-53; Ex. 1003, ¶127. Panescu discloses that each switch in the ASIC includes a "PMOS transistor." Ex. 1008, 10:50-53; Ex. 1003, ¶130. Accordingly, Panescu discloses "*transistor switches*" that are "*are selected from the group consisting of PMOS or MOS transistors*." Ex. 1003, ¶130.

Both Panescu and Hitzelberger are analogous art to the '298 patent because each is in the field of electrode stimulation. Ex. 1001, 1:11-14; Ex. 1005, 1; *see also* Ex. 1005, 4; Ex. 1008, 1:16-21; Ex. 1003, ¶132. Moreover, Panescu is analogous because it is reasonably pertinent to a problem mentioned in the '298 patent: namely, to conserve space taken up by circuitry. Ex. 1001, 1:49-51; Ex. 1008, 2:64-68; Ex. 1003, ¶132.

It would have been obvious to use Panescu's switches made up of PMOS transistors in place of Hitzelberger's switches. Ex. 1003, ¶133. This would have been simply an arrangement old elements (*i.e.*, switches made up of PMOS transistors) with each performing the same function it had been known to perform (*i.e.*, electronic switching) and yielded no more than one would expect from such an arrangement. *Id.* Thus, it would have been obvious. *KSR Intl Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

D. Claims 1-5 and 11-14 Are Obvious Over Panescu (Ex. 1008) in view of Faltys (Ex. 1009)

1. Overview of Panescu (Ex. 1008) and Faltys (Ex. 1009)

U.S. Patent No. 6,101,410 to Panescu et al. ("Panescu") (issued on August 8, 2000; prior art under 35 U.S.C. § 102(b) (pre-AIA)) discloses a cardiac mapping and pacing system that uses multiple electrodes for stimulation and recording data. Ex. 1008, Abstract, 1:16-21. More specifically, Panescu discloses an application specific integrated circuit (ASIC) that uses a CMOS switching matrix to connect a number of individual electrodes with either a biological recorder or external pacing stimulators. Ex. 1008, Abstract, 7:8-14; Ex. 1003, ¶134.

U.S. Patent No. 6,219,580 to Faltys et al. ("Faltys") (issued on April 17, 2001; prior art under 35 U.S.C. § 102(b) (pre-AIA)) discloses an implantable cochlear system that provides "selected pulsatile stimulation" using electrodes. Ex. 1009, Abstract, 4:16-18; *see also* Ex. 1009, 4:50-54. Each electrode use DACs

to provide it current for stimulation. Ex. 1009, 31:20-25; Ex. 1003 ¶135. Thus, multiple DACs "drive the stimulation electrodes." Ex. 1009, 26:11-12.

2. Claim 1

i. *Preamble*

Claim 1 recites "*[a] stimulation output switching system for a multi-channel stimulator, said system comprising: …."* Panescu discloses this limitation. Ex. 1003, ¶¶136-140.

Panescu discloses an invention that relates to an "application specific integrated circuit (ASIC) operable to configure multiple input electrodes for cardiac signal recording and analysis or stimulation based on the immediate necessities of a particular electrophysiological procedure." Ex. 1008, 1:16-21. In other words, Panescu's ASIC uses cardiac electrodes for measurement or stimulation. Ex. 1003, ¶137; Ex. 1008, 1:16-21. For stimulation, Figure 1 of Panescu shows a system that has "two external pacing pulse generators or stimulators 36" (shown in blue) connected to multiple cardiac electrodes 16 and 17 (shown in green), shown below:

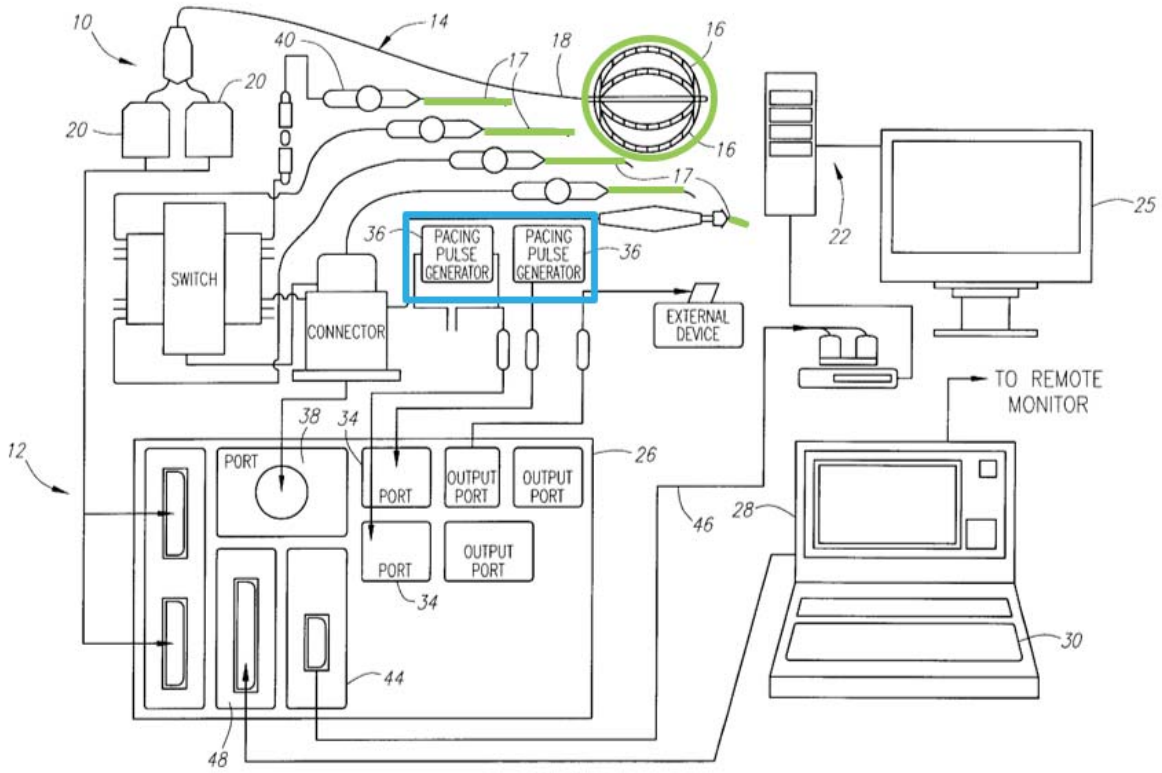


FIG. 1

Ex. 1008, Fig. 1 (annotated) 6:19-21 ("ports 34 are provided for connection to … stimulators 36."); Ex. 1003, ¶137.

Panescu further discloses that the pulse generators 36 may provide stimulation to any of the cardiac electrodes 16 and 17 shown above. Ex. 1008, 6:22-24 ("Pacing pulses generated by the external pacing pulse stimulators 36 can be selectively coupled to any of the available cardiac electrodes 16 and 17 to permit cardiac pacing through any of the electrodes 16 and 17."); Ex. 1003, ¶138. To do so, Panescu's ASIC uses switches to select the appropriate pulse generator connection and electrodes. Ex. 1008, 2:20-26; Ex. 1003, ¶138; *see also* Ex. 1008, 7:8-14 ("The control/core logic circuit 57 … configures the cross point switch

matrix so as to establish desired electrical connections between the various electrodes, the external pacing stimulators 36 and the biological recorder 22.”). Figure 5 of Panescu shows the pacing mode circuitry (*i.e.*, stimulation mode) with the external stimulators (blue box) connected to switches (yellow box) for each electrode input (green box), shown below:

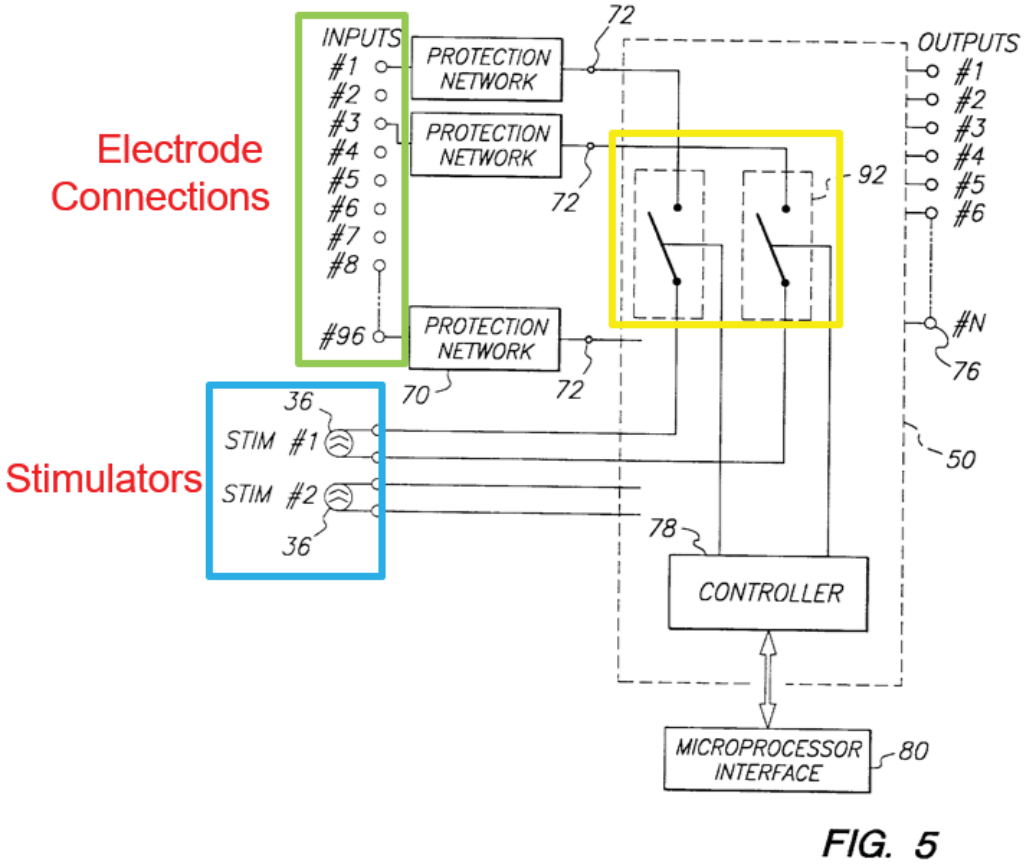


FIG. 5

Ex. 1008, Fig. 5 (annotated), 8:65-9:2; Ex. 1003, ¶139. Panescu discloses that these switches “permit[] pacing pulses generated by any of the external stimulators 36 to be applied to the heart through any of the cardiac electrodes 16, 17.” Ex. 1008, 6:65-68.

Based on these teachings, Panescu discloses a switching system for stimulation of multiple electrodes at different stimulation parameters, *i.e.*, a "*stimulation output switching system for a multi-channel stimulator*." Ex. 1003, ¶140.

ii. *N DACs*

Claim 1 also recites *"N number of DACs (11)."* Figure 5 of Panescu illustrates four stimulation input terminals (shown in red) used to stimulate electrodes, shown below:

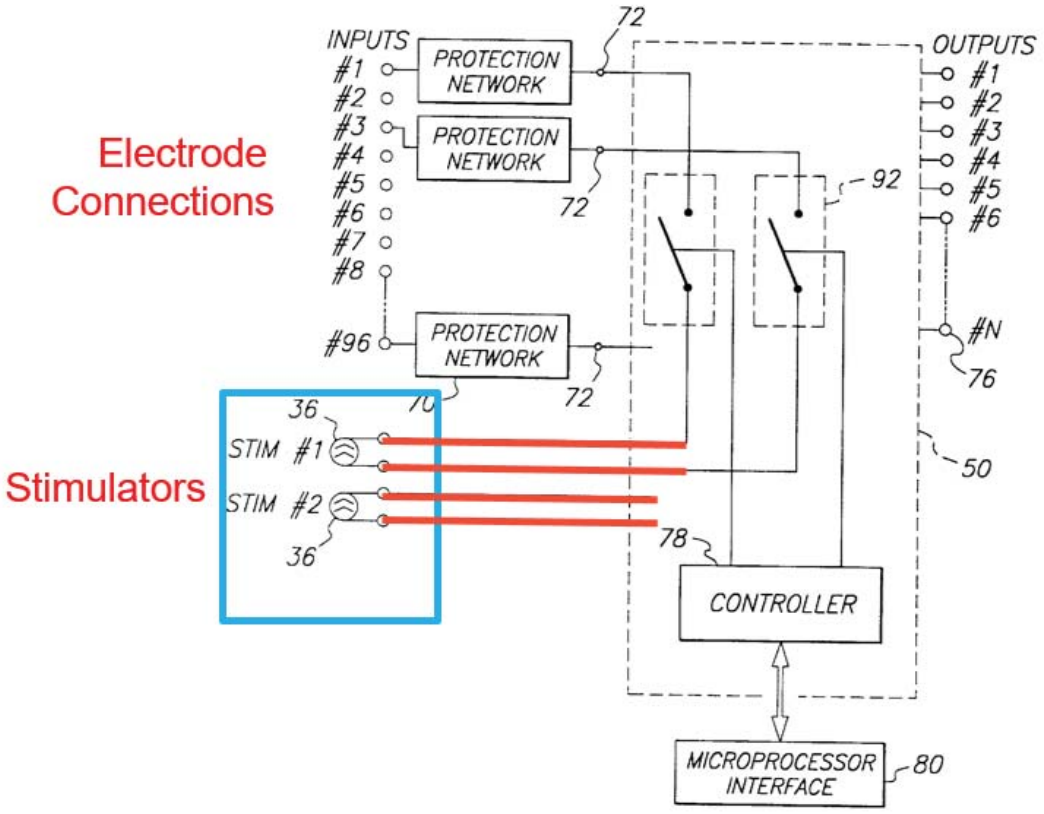


FIG. 5

Id., Fig. 5, 8:65-9:2; Ex. 1003, ¶142. These four terminals provide pacing pulses to any cardiac electrodes. Ex. 1008, 6:21-24, 6:54-58; *see also* Ex. 1008, Fig. 3 ("External stimulator Inputs (4) 55"); Ex. 1003, ¶142. Accordingly, Panescu has four different input terminals used to provide stimulating pulses to electrodes. Ex. 1003, ¶142.

Panescu does not expressly use "*DACs*" to stimulate electrodes. Using DACs to stimulate electrodes, however, was well known by 2002. *E.g.*, Ex. 1005, Fig. 5; Ex. 1006, 1212, Figs. 1 and 2. For example, Faltys discloses a system that provides "selected pulsatile stimulation" using electrodes. Ex. 1009, 4:16-18, 4:50-54. "Each electrode has its own current mode DAC 420 and 422…" *Id.*, 31:20-25. The DAC provides a source or sink current to the electrode. *Id.*, 26:23-25; Ex. 1003, ¶144. Faltys further discloses that the DACs "drive the stimulation electrodes." Ex. 1009, 26:11-12. These DACs are controlled by a code word that provides the pulse shape and timing used for stimulation. *Id.*, 25:49-59; Ex. 1003, ¶144. Accordingly, Faltys discloses using "*DACs*" to stimulate electrodes. Ex. 1003, ¶144.

It would have been obvious to a POSA to have used "*DACs*" to stimulate the electrodes in Panescu. Ex. 1003, ¶145. Specifically, it would have been obvious to use four "*DACs*"—one for each of the four input terminals—to drive Panescu's electrodes. Ex. 1003, ¶145.

As explained above, *see* §VI.C, Panescu is analogous art to the '298 patent. *See* Ex. 1003, ¶132. Similarly, Faltys is analogous art to the '298 patent because each is in the field of electrode stimulation. Ex. 1001, 1:11-14; Ex. 1009, 1:25-28; Ex. 1003, ¶146. Moreover, Faltys is also analogous for being reasonably pertinent to a different problem faced by the inventors of the '298 patent, *i.e.*, providing higher resolution in cochlear applications for. Ex. 1001, 1:34-36; Ex. 1009, 7:42-48; Ex. 1003, ¶146.

It would have been obvious to use individual DACs, as described by Faltys, to drive each of Panescu's four input terminals thereby stimulating electrodes. Ex. 1003, ¶147. A skilled artisan would have recognized that DACs provide the added benefit of different stimulation waveforms. Ex. 1003, ¶147. For example, Falty's discloses that the DACs can have different pulse amplitudes, pulse shapes, and pulse timing. Ex. 1009, 26:11-14, 25:49-67; *see also id*., 15:62-16:2; Ex. 1003, ¶147. Thus, using DACs to stimulate electrodes allows a user to configure different stimulation waveforms for delivery to multiple electrodes simultaneously as needed. Ex. 1003, ¶147.

Moreover, it would have been obvious to use DACs to stimulate Panescu's electrodes as it is simply an arrangement old elements (*i.e.*, DACs) with each performing the same function it had been known to perform (*i.e.*, stimulating electrodes) and yields no more than one would expect from such an arrangement. Ex.

1003, ¶148; *KSR*, 550 U.S. at 417. Notably, the '298 patent expressly states that the "conventional" prior art used DACs to stimulate electrodes, thereby showing this use of DACs was well-known. Ex. 1001 3:66-4:1; Ex. 1003, ¶148; *see also id.*, Fig. 2, 3:54-4:3. This is confirmed by Faltys' system, which also uses DACs to stimulate electrodes. Ex. 1009, 26:11-12; Ex. 1003, ¶148. A skilled artisan would have recognized that using DACs to stimulate Panescu's electrodes would yield no more than one would expect, *i.e.*, using DACs to stimulate electrodes. Ex. 1003, ¶148. Accordingly, the combination of Panescu and Faltys would have been obvious. Ex. 1003, ¶148

Thus, it would have been obvious to use individual DACs, as described by Faltys, to drive each of Panescu's four input terminals, thereby stimulating the electrodes. This combination of Panescu and Faltys thus discloses "*N number of DACs*," where N = 4. Ex. 1003, ¶149.

iii. *M Electrode Contacts*

Claim 1 also recites *"M number of electrode contacts (31) …."* The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶150-154.

Figure 5 of Panescu discloses that there are 96 input pins:

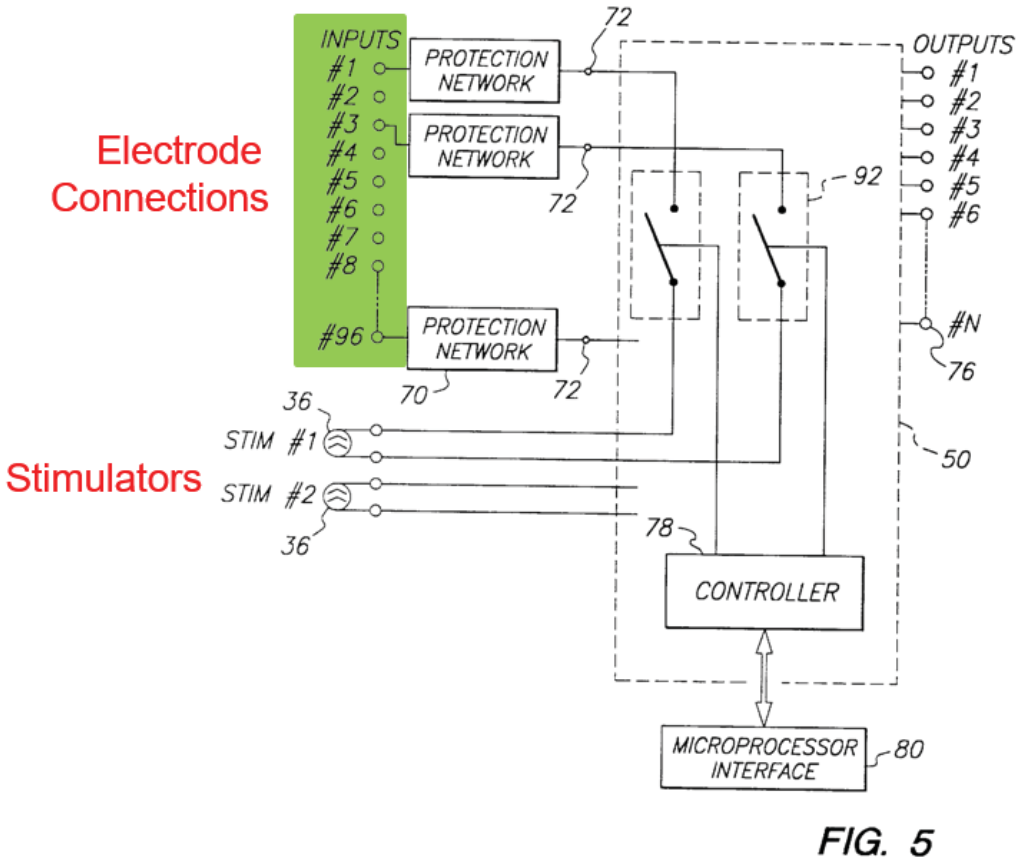


FIG. 5

Ex. 1008, Fig. 5 (annotated), 6:51-54 ("ASIC 50 … includes ninety-six primary analog input pins 52 and seventy-two analog output pins 54."); Ex. 1003, ¶151.

Each of these input pins may be connected to an electrode ("*electrode contacts*") for stimulation: "Each of the Switches 92 can be separately actuated under the control of the controller 78 to couple the principal terminals of either stimulator 36 to any pair of input pins 72 and thus, to any pair of electrodes connected to those particular input pins 72." Ex. 1008, 8:65-9:2; Ex. 1003, ¶152. In particular, these input pins allow pacing pulses to reach the cardiac electrodes

16 and 17. Ex. 1008, 6:63-67; Ex. 1003, ¶152. Accordingly, each input pin may be connected to a single electrode. Ex. 1003, ¶152. Thus, Panescu discloses an ASIC that supports up to 96 cardiac electrodes ("*electrode contacts*").

For example, in the configuration where Panescu's ASIC used 96 cardiac electrodes, all 96 input pins would be connected to an electrode. Ex. 1003, ¶153. In that case, every input pin corresponds to an individual electrode. *Id.* Accordingly, Panescu's ASCI would have "*M number of electrode contacts*," where M = 96. *Id.*

The combination of Panescu and Faltys thus discloses "*M number of electrode contacts*," where M = 96. *Id.*, ¶154.

iv. *NxM Switches*

Claim 1 additionally recites *"NxM number of switches (21)."* The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶155-158. Panescu discloses that there is one switch for every electrode and stimulator 36 input line: "Each of the input pins 90 is coupled through a separate, individual, controllable switch 92 to each of the input pins 72." Ex. 1008, 8:63-9:2. "Each of the switches 92 can be separately actuated under the control of the controller 78 to couple the principal terminals of either stimulator 36 to any pair of input pins 72 and thus, to any pair of electrodes connected to those particular input pins 72." *Id.*; Ex. 1003, ¶156.

As explained above, *see* §VI.D.2.ii and VI.D.2.iii, Panescu's ASIC has four input terminals and 96 input pins. Panescu discloses that this configuration would have 384 switches that connect each input terminal to every single electrode. Ex. 1003, ¶157. As combined with Faltys, and as shown in §§VI.D.2.ii and VI.D.2.iii, Panescu would have four DACs (*i.e.*, N = 4) supporting 96 electrodes (*i.e.*, M = 96). Thus, 384 switches is "*NxM number of switches*" as there are four DACs supporting 96 electrodes, *i.e.*, 4 x 96 = 384. Ex. 1003, ¶157.

The combination of Panescu and Faltys therefore discloses "*NxM number of switches*" by disclosing 384 switches.

v. *DAC to Switch Coupling*

Claim 1 also recites "*wherein each DAC (11) of the N number of DACs is coupled uniquely to one group (50) of M number of switches (21).*" The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶159-163.

Figure 5 of Panescu shows 2 switches that are each uniquely coupled to one of the input terminals (*i.e.*, the red or orange group), shown below:

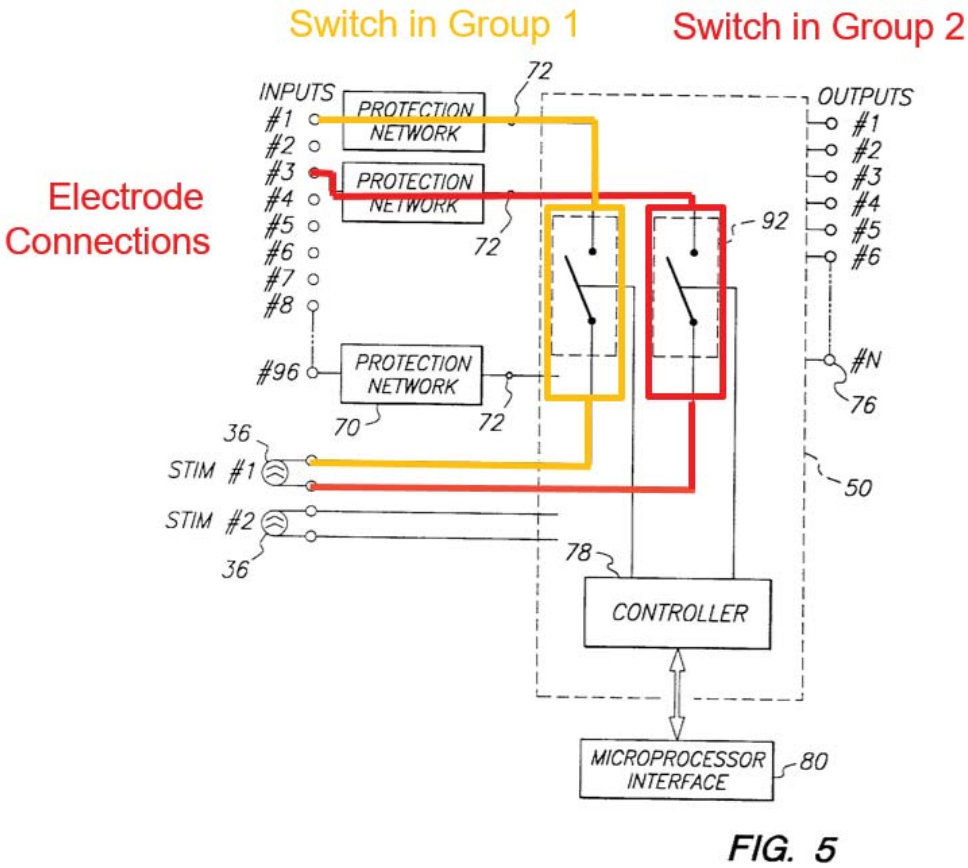


FIG. 5

Figure 5 (annotated), 8:65-9:2; Ex. 1003, ¶160. In addition, there would be 2 other switch groups (not shown) connected to the other input terminals (shown as terminals to STIM # 2 above). Ex. 1003, ¶160.

As explained above, *see* §VI.D.2.iv, there are 384 switches described in the circuit of Figure 5. Of those, 96 switches are connected to each input terminal. Ex. 1003, ¶161. Accordingly, Panescu's ASIC has 4 groups of 96 switches ("*one group of the M number of switches*") with each group connected to an input terminal. Ex. 1008, 8:63-9:2; Ex. 1003, ¶161. Panescu's ASIC, as combined with Faltys, would have 4 DAC switch groups, each of which is connected to an

individual DAC ("*wherein each DAC of the N number of DACs is coupled uniquely*" to a switch group). Ex. 1003, ¶162. Accordingly, the combined system of Panescu and Faltys discloses 4 DAC switch groups with each having 96 switches. Ex. 1003, ¶162

The combination of Panescu and Faltys therefore discloses four switch groups of ninety-six switches that are each connected to one of the four DACs ("*wherein each DAC of the N number of DACs is coupled uniquely to one group of the M number of switches*"). Ex. 1003, ¶163.

vi. *Switch to Electrode Contact Coupling*

Claim 1 additionally recites *"each switch within each group (50) of M switches, in turn, is coupled to each one of M electrode contacts (31)."* The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶164-166.

Panescu discloses that each switch connects the input terminals to an individual electrode: each switch 92 couples "the principal terminals of either stimulator 36 to… any pair of electrodes connected to those particular input pins 72." Ex. 1008, 8:63-9:2; *see also* Ex. 1008, 7:8-14 ("the cross point switch matrix … establish[es] desired electrical connections between various electrodes…."); Ex. 1003, ¶165. Each switch is thus connected to one electrode contact. Ex. 1003, ¶165. Accordingly, and as combined, Panescu discloses that each switch 92 is connected to a single electrode and one DAC ("*each switch within each group of*

M switches, in turn, is coupled to each one of M electrode contacts."). Ex. 1003, ¶165.

vii. *Wherein Clause*

Claim 1 also recites "*wherein M and N are whole numbers and M is greater than N.*" The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶167-169.

As explained above, *see* §§VI.D.2.ii and VI.D.2.iii, the combined system of Panescu and Faltys has 4 DACs and 96 electrode contacts. Accordingly, N = 2 ("*N number of DAC*s") and M = 96 ("*M number of electrode contacts*"). Ex. 1003, ¶168. 4 and 96 are whole numbers and 96 is greater than 4. Ex. 1003, ¶168.

3. Claims 2 and 3

Claim 2 recites "*[t]he system of claim 1 wherein the switches are transistor switches*," and claim 3 recites "*[t]he system of claim 2 wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors.*" The combination of Panescu and Faltys discloses these limitations. Ex. 1003, ¶¶170-174.

Panescu discloses that each switch in the ASIC includes a "PMOS transistor." Ex. 1008, 10:50-53 ("As illustrated, each switch 74 includes a PMOS transistor 150 having its principal electrodes connected in parallel with the principal electrodes of an NMOS transistor 152."); Ex. 1003, ¶171. Thus, the

switches in Panescu's ASIC are "*transistor switches*," and specifically include PMOS transistors. Ex. 1003, ¶¶171, 174; *see also* Ex. 1008, 10:48-65.

4. Claim 4

Claim 4 recites "*[t]he system of claim 1 wherein the switches are programmable using software or hardware programming.*" The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶¶175-178.

Panescu discloses that the switches are "actuated under the control of controller 78." Ex. 1008, 8:65-9:2, Fig. 5; Ex. 1003, ¶176. Panescu further discloses that controller 78 is "controlled by a microprocessor interface 80." Ex. 1008, 8:39-41. To do so, the microprocessor issues commands to the microprocessor interface. Ex. 1003, ¶177; Ex. 1008, 9:2-5. Panescu's ASIC is controlled using these commands, which are *software programming*. *See* Ex. 1003, ¶177; Ex. 1008, 11:48-12:24. For example, an applied switching command tells the ASIC to activate a switch. Ex. 1008, 11:59-62; Ex. 1003, ¶177. Accordingly, Panescu's switches are programmable using software commands ("*wherein the switches are programmable using software or hardware programming*").

5. Claim 5

Claim 5 recites "*[t]he system of claim 4, wherein the programming allows one and only one switch (21), at any one time, to be electrically closed (connected)*

to one particular electrode contact (31), and thereby permit current to flow through that single electrode contact." The combination of Panescu and Faltys discloses this limitation. Ex. 1003, ¶179-181.

Panescu discloses that each switch is individually controllable and toggled based on an applied switching command. Ex. 1008, 7:7-14. This includes establishing the "desired electrical connections between the various electrodes" and "the external pacing stimulators." *Id.*; Ex. 1003, ¶180. Panescu also explains that the "control circuit … control[s] the cross point switch matrix to couple selected ones of the inputs with selected ones of the outputs." Ex. 1008, 2:35-42. As explained above, *see* §VI.D.2.vi, each switch is also connected to a single electrode. Ex. 1003, ¶180. Accordingly, Panescu's ASIC programming described above can therefore, *at any one time*, operate a single switch to connect ("*electrically closed (connected)*") and stimulate a single electrode ("*permit current to flow through that single electrode contact*") while leaving the other electrodes disconnected. Ex. 1003, ¶180.

6. Claim 11

Claim 11 is rendered obvious by Panescu and Faltys for the same reasons described above for claim 1. Specifically, Panescu as combined with Faltys disclose *"[a] method of switching outputs in a multi-channel stimulator, said method comprising:"* (§ VI.D.2.i) *"(a) providing N number of DACs (11)"* (§

VI.D.2.ii), *"(b) providing M number of electrode contacts (31)"* (§ VI.D.2.iii) *"(c) coupling each of N DACs (11) to a group of M switches (31)"* (§§ VI.D.2.iv-v) *"(d) coupling each of the M switches (31) uniquely to each of M electrode contacts (31)"* (§ VI.D.2.vi), and *"wherein M and N are whole numbers and M is greater than N"* (§ VI.D.2.vii). Ex. 1003, ¶¶182-186, 188.

Panescu as combined with Faltys further discloses *"(e) connecting selected Switches (21) by closing the Switches, to electrically connect selected electrode contacts (31) to transmit current, while avoiding closing more than one Switch (21) connected to the same electrode contact (31) at any one time, wherein there is at least NxM total number of switches (31) …."* As explained above with respect to claim 5 (§ VI.D.5), Panescu's ASIC programming can, at any one time, operate a single switch to electrically connect and stimulate a single electrode while leaving the other electrodes disconnected. Ex. 1008, 2:35-42, 7:7-14; Ex. 1003, ¶180. Panescu also discloses that, when an electrode is stimulated, the signal "is used to inhibit switching of the cross point switch matrix…." Ex. 1008, 7:44-47.

7. Claims 12 and 13

Claim 12 recites *"[t]he method of claim 11 wherein the switches are transistor Switches*" and claim 13 recites *"[t]he method of claim 12 wherein the transistor switches are selected from the group consisting of PMOS or MOS*

transistors." The combination of Panescu and Faltys discloses these limitations for the same reasons provided for claims 2 and 3. Ex. 1003, ¶¶189-190.

8. Claim 14

Claim 14 recites *"[t]he method of claim 11 wherein the step (e) of connecting [s]witches is accomplished by using software or hardware programming."* The combination of Panescu and Faltys discloses this limitation for the same reasons provided for claim 4. Ex. 1003, ¶191.

E. Claims 6-10 and 15-19 are anticipated by Jones (Ex. 1006)

1. Overview of Jones

K. Jones and R. Normann, "*An Advanced Demultiplexing System for Physiological Stimulation,"* IEEE Transactions on Biomedical Engineering, 44(12): 1210-1220 (1997) ("Jones") (Ex. 1006) is a paper that was published by the IEEE in 1997. The IEEE is a well-known organization that publishes articles, organizes conferences, and establishes standards. Ex. 1003, ¶¶62-64; *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 11 (PTAB May 18, 2015) ("IEEE is a well-known, reputable compiler and publisher of scientific and technical publications."). Jones identifies that it was published in December 1997 as part of the IEEE Transactions on Biomedical Engineering, Vo. 44, No. 12. Ex. 1006, Cover, 1210. The specific copy of Jones filed as Exhibit 1006 was further date-stamped on December 9, 1997, by the UCLA Science & Engineering Library.

Id., Cover; Ex. 1003, ¶¶195-196. Jones was therefore published and disseminated to the public by 1997, and is prior art under 35 U.S.C. § 102(b) (pre-AIA). *See also* Ex. 1014, 260 (citing Jones as reference [17]); Ex. 1023, 70 (same for reference [6]).

Jones describes a "CMOS very large scale integration (VLSI) chip … designed and built to implement a scheme developed for multiplexing / demultiplexing the signals required to operate an intracortical stimulating electrode array." Ex. 1006, 1210. Jones recognizes that "[b]y incorporating multiple current sources on chip, many channels may be stimulated simultaneously." *Id.* Jones describes an eight-channel stimulator that is "scalable to a 625-channel stimulator." *Id.*; Ex. 1003, ¶192.

Jones explains that "the area taken up by the DAC's (and their associated circuitry)" means "it may not be practical to employ one DAC per electrode on the chip." Ex. 1006, 1211; Ex. 1003, ¶193. But "this many DAC's would not be required" according to Jones because "[i]t should not, in general, be necessary to pass current through all channels simultaneously …." Ex. 1006, 1211. Instead, "it is possible to time-demultiplex the pulses coming from a DAC, and use one DAC to stimulate a number of electrode sites." *Id.*

Jones describes a system with multiple DACs, with one DAC "for each eight channels (electrodes) to be serviced." *Id.*, 1212. This is illustrated in Figure 1:

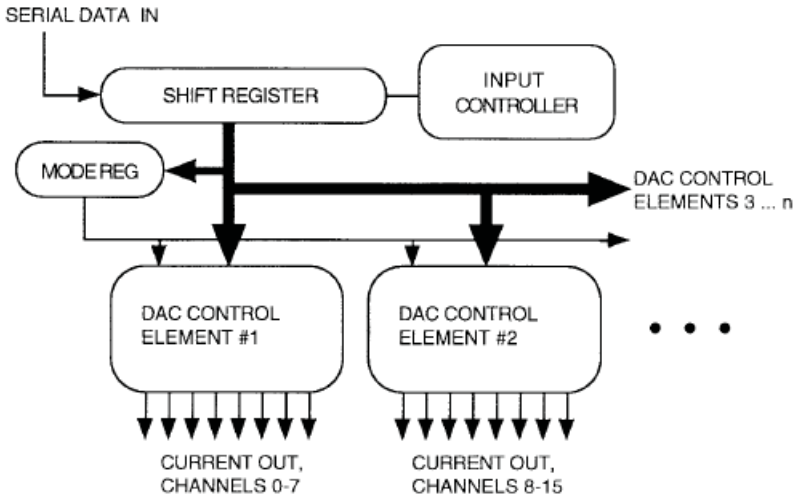


Fig. 1. Chip architecture. DAC control element architecture is diagrammed in Fig. 2.

Ex. 1006, Fig. 1; Ex. 1003, ¶194. Each of the DACs work with "DAC Demultiplexer/Passgates," a "set of eight CMOS passgates" which are switches that "determine which of the eight channels is active" and thereby control which corresponding electrodes are stimulated. Ex. 1006, 1216; Ex. 1003, ¶194.

2. Claim 6

i. *Preamble*

Claim 6 recites *"[a] stimulation output switching system for a multichannel stimulator."* Jones discloses this limitation. Ex. 1003, ¶¶197-199.

Jones' system can "control a large quantity (up to several hundred) of stimulating electrodes" and is "implemented as an eight-channel stimulator, [and] is scalable to a 625-channel stimulator…." Ex. 1006, 1210 (Abstract). Jones' chip architecture has an input section and multiple DAC subsystems (containing "*a stimulation output switching system*"), as shown in Figure 1 below:

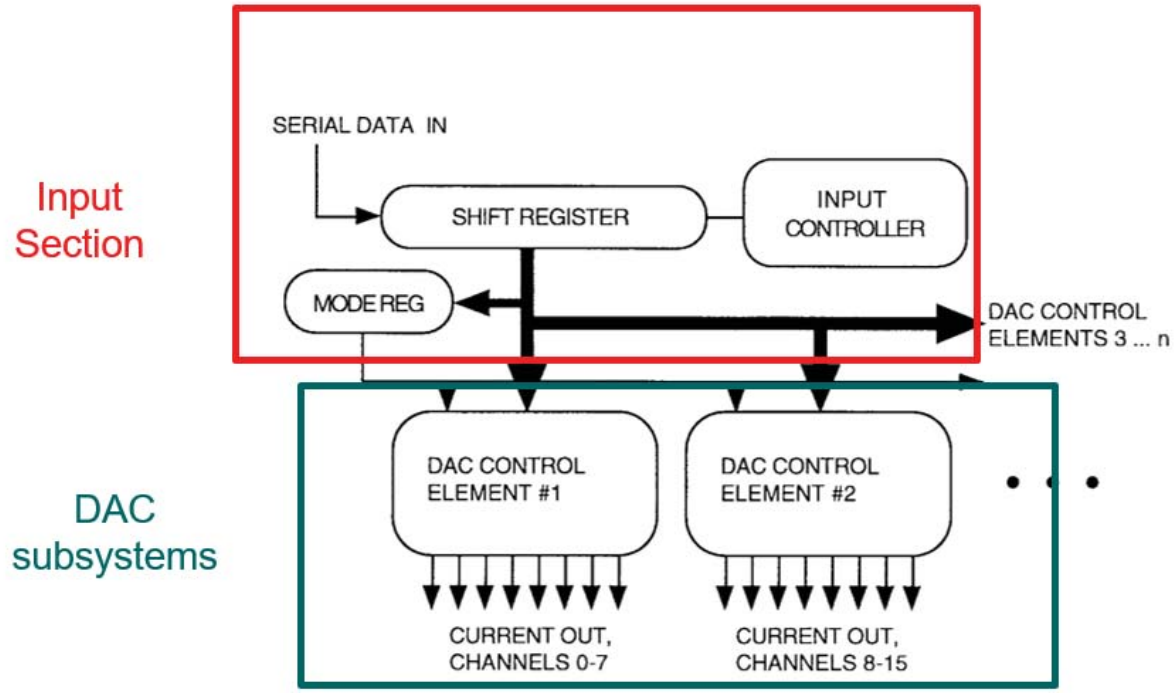


Fig. 1. Chip architecture. DAC control element architecture is diagrammed in Fig. 2.

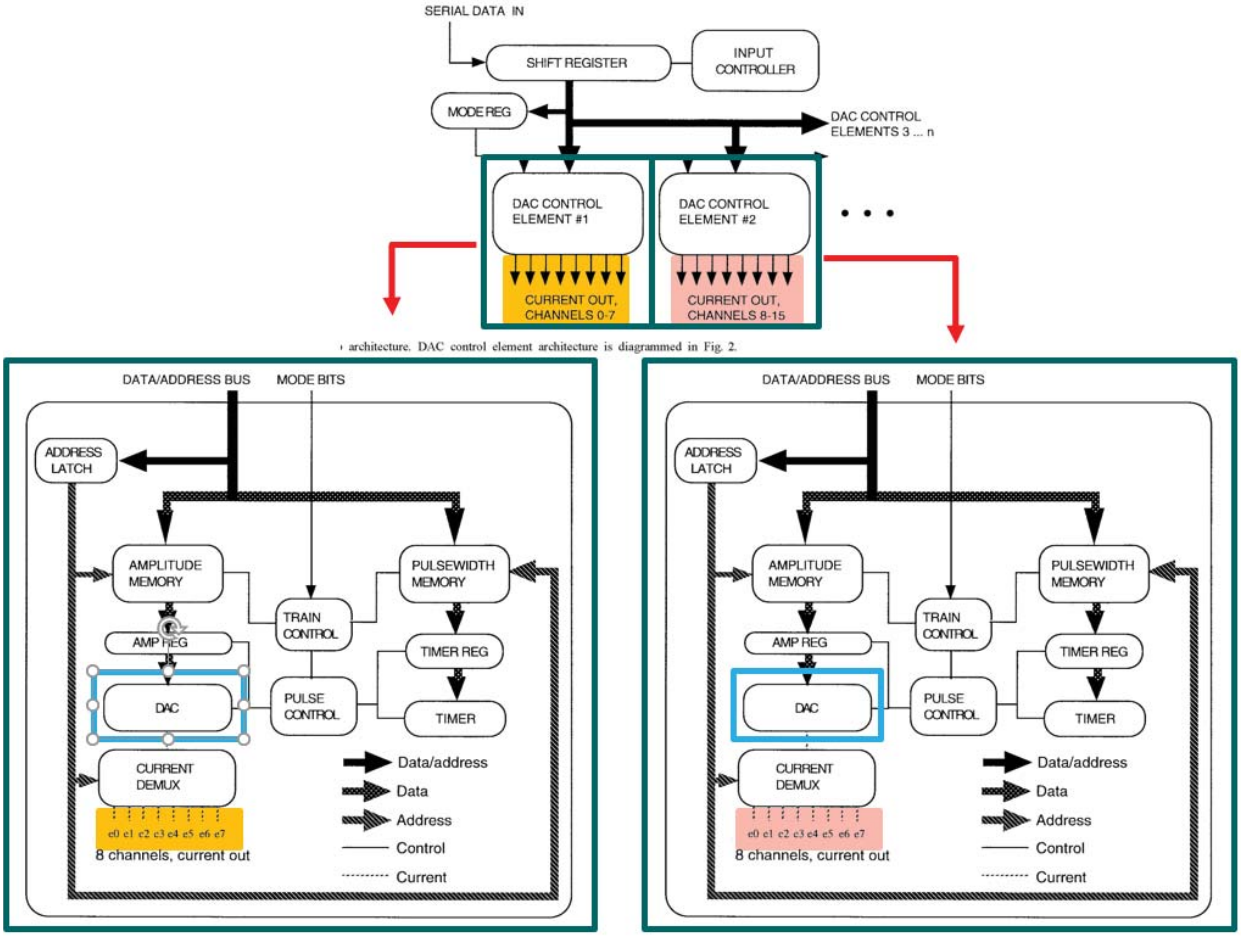
Ex. 1006, Fig. 1 (annotated), 1211. Jones' "the architecture … may be divided into two sections: [t]he input section, of which there will be one per chip, and the DAC subsystems, … one for each eight channels (electrodes)." *Id.*; Ex. 1003, ¶198.

Jones further discloses that the system is a "*multichannel*" stimulator. Ex. 1003, ¶199. For example, Jones discloses that the system uses multiple current sources that allows "many channels [to] be stimulated simultaneously" with different stored "waveform parameters." Ex. 1006, 1210 (Abstract), 1212. Based on this disclosure, Jones discloses a "*multichannel stimulator*." Ex. 1003, ¶199.

ii. *N DACs*

Claim 6 also recites "*N number of DACs (12).*" Jones discloses this limitation, specifically that that N = 2. Ex. 1003, ¶¶200-202.

As shown above, Figure 1 of Jones shows two DAC subsystems (referred to as "DAC control elements" in Figures 1 and 2). Ex. 1006, Figs. 1, and 2, p1213. As shown below, each DAC subsystem has a "DAC current source" (blue boxes) and has "eight channels (electrodes) to be serviced" (orange and pink boxes):



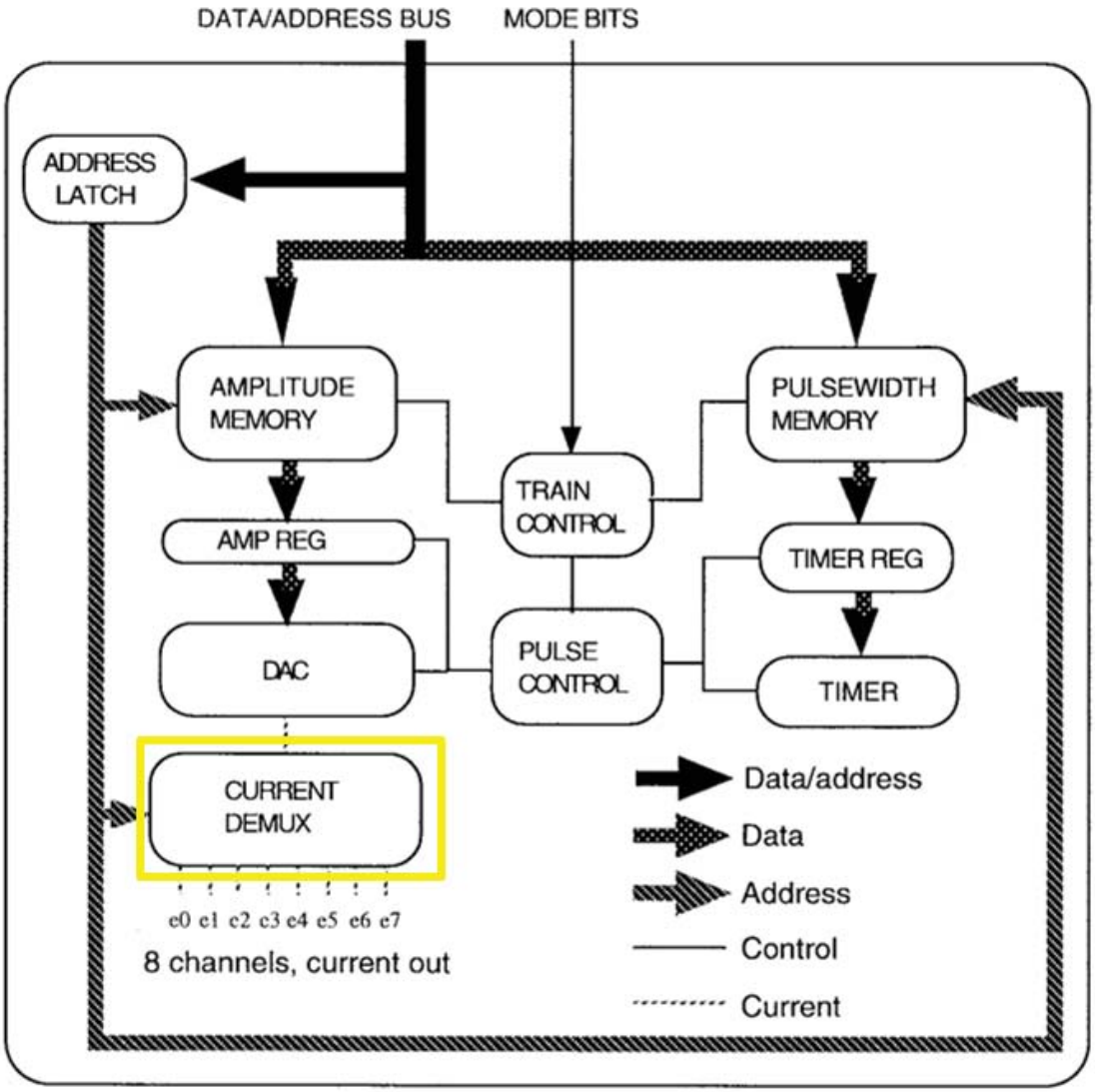
Ex. 1006, 1212, Figs. 1 and 2 (annotated); Ex. 1003, ¶201.

As shown above, Figure 1 of Jones shows 2 DAC subsystems (*i.e.*, "DAC Control Element #1" and "DAC Control Element #2") thereby showing 2 DAC

current sources (shown in red boxes above). Ex. 1003, ¶202. Accordingly, Jones discloses "*N number of DACs*" where N = 2.

iii. *M Switches in N Grouped Sets of L Switches*

Claim 6 also recites "*M number of switches (121), grouped into N grouped sets (110) of switches, each set (110) having L number of switches (121).*" Jones discloses this limitation, specifically that M = 16, N = 2 (as discussed above), and L = 8. Ex. 1003, ¶203-209. Each DAC Control element has a DAC Demultiplexer/Passgate (referred to as a "Current Demux" in Figure 2):



Ex. 1006, Fig. 2 (annotated), 1216 ("2) DAC Demulitplexer/Passgates:…"); Ex. 1003, ¶204.

The "Current Demux" component is a "set of eight CMOS passgates" ("*switches*") "selected by a three-to-eight decoder…." Ex. 1006, 1216; Ex. 1003, ¶205; Ex. 1006, 1216. "The passgates determine which of the eight channels is active, and also connect all of the unused channels to the exhaust line." Ex. 1006,

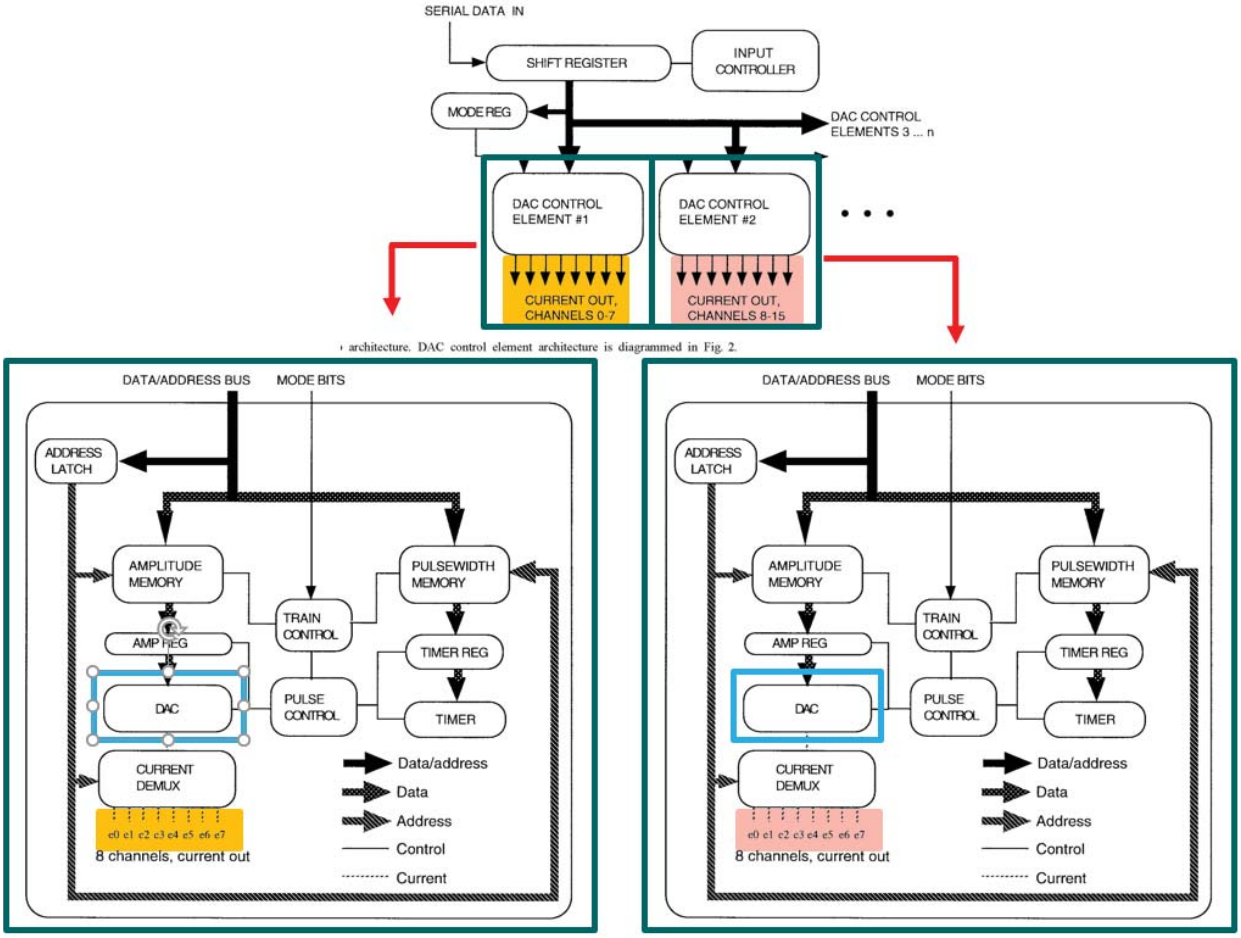
1216. Accordingly, there are 8 CMOS passgates ("*switches*") per DAC control element. Ex. 1003, ¶205. Jones' 2 DAC control elements would thus have a total of 16 CMOS passgates ("*M number of switches*"), or 8 each ("*each set having L number of switches*"). Ex. 1006, 1216, Figs. 1 and 2 (annotated in § VI.E.2.ii), Ex. 1003, ¶206. Jones thus discloses "*M number of* switches" where M = 16.

As shown above, the annotated Figure also shows that each DAC has its own set of 8 CMOS passgates connected to electrodes in the orange and pink boxes (the switches are "*grouped into N grouped sets of switches*" as N = 2). Ex. 1003, ¶208. Accordingly, the 16 CMOS passgates are divided into 2 groups: an orange switch group and pink switch group. Ex. 1003, ¶208. Further, both sets of switches above each have 8 switches. Ex. 1003, ¶208. Thus, Jones discloses "*each set (110) having L number of switches*," where L = 8. Ex. 1003, ¶208.

iv. *M Electrode Contacts*

Claim 6 also recites *"M number of electrode contacts (130)."* Jones discloses this limitation, specifically that M = 16. Ex. 1003, ¶¶210-212.

As shown above, Figure 1 of Jones shows 2 DAC control elements. Ex. 1006, Figs. 1 and 2, p1213. Each DAC control element (blue boxes) has "eight channels (electrodes) to be serviced" (orange and pink boxes) shown below:



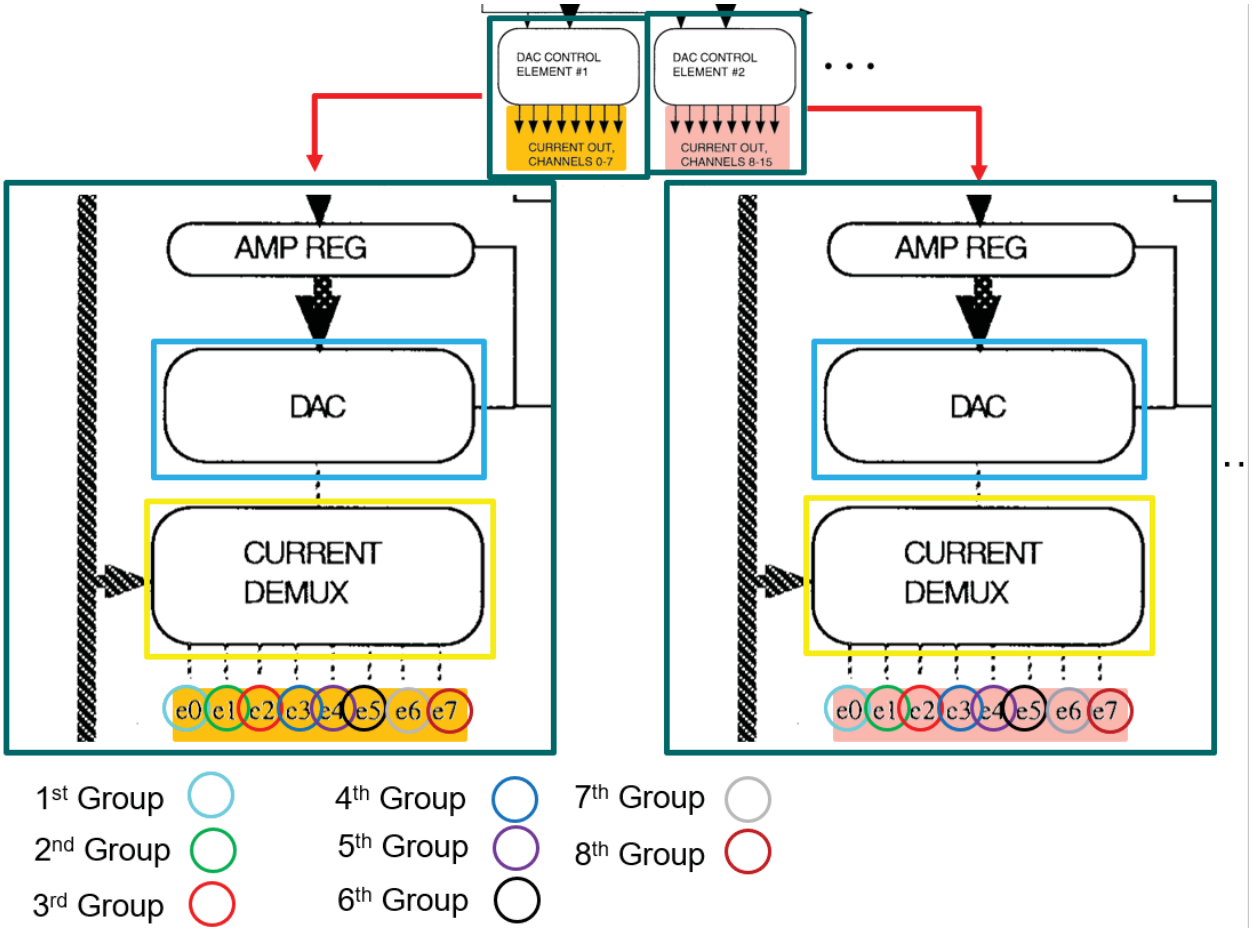
Ex. 1006, 1212, Figs. 1 and 2 (annotated); Ex. 1003, ¶211.

Accordingly, there are a total of 16 electrodes shown in the 2 DAC control elements of Figure 1 of Jones. Ex. 1003, ¶212. Jones therefore discloses "*M number of electrode contacts*" where M = 16.

v. *L Electrode Contact Groups* (Limitation 6[d])

Claim 6 also recites "*L number of electrode contact groups (100).*" Jones discloses this limitation, specifically that L = 8. Ex. 1003, ¶¶213-219. Jones discloses 8 different groups of electrodes, specifically a first group of the first

electrode in each DAC control element, a second group of the second electrode in each DAC control element, etc.:



Ex. 1006, Figs. 1 and 2 (annotated). Each of these groups of electrodes contains multiple electrodes and, as explained below, may be stimulated at the same time. Ex. 1003, ¶214.

Jones discloses a chip architecture that has a 7-bit address used to access each DAC and its corresponding channels. Ex. 1006, 1215 ("A 7-b address is used to access all channels and registers on the chip."). Jones uses different bits to provide different instructions to the DACs in a system. Ex. 1006, 1215; Ex. 1003,

¶215. One bit, a_6, indicates whether the instruction is "normal" or "special." Ex. 1006, 1215; Ex. 1003, ¶215. Jones discloses that the least significant bits—*i.e.*, a_1 a_0— are used to "select an individual DAC in the chip." Ex. 1006, 1215; Ex. 1003, ¶216. When a_1 a_0 are set equal to "11," the chip architecture accesses all DACs. Ex. 1006, 1215; Ex. 1003, ¶216. Accordingly, Jones' disclosure would enable the chip architecture to access all DACs simultaneously when a_1 a_0 are set to "11." Ex. 1003, ¶216.

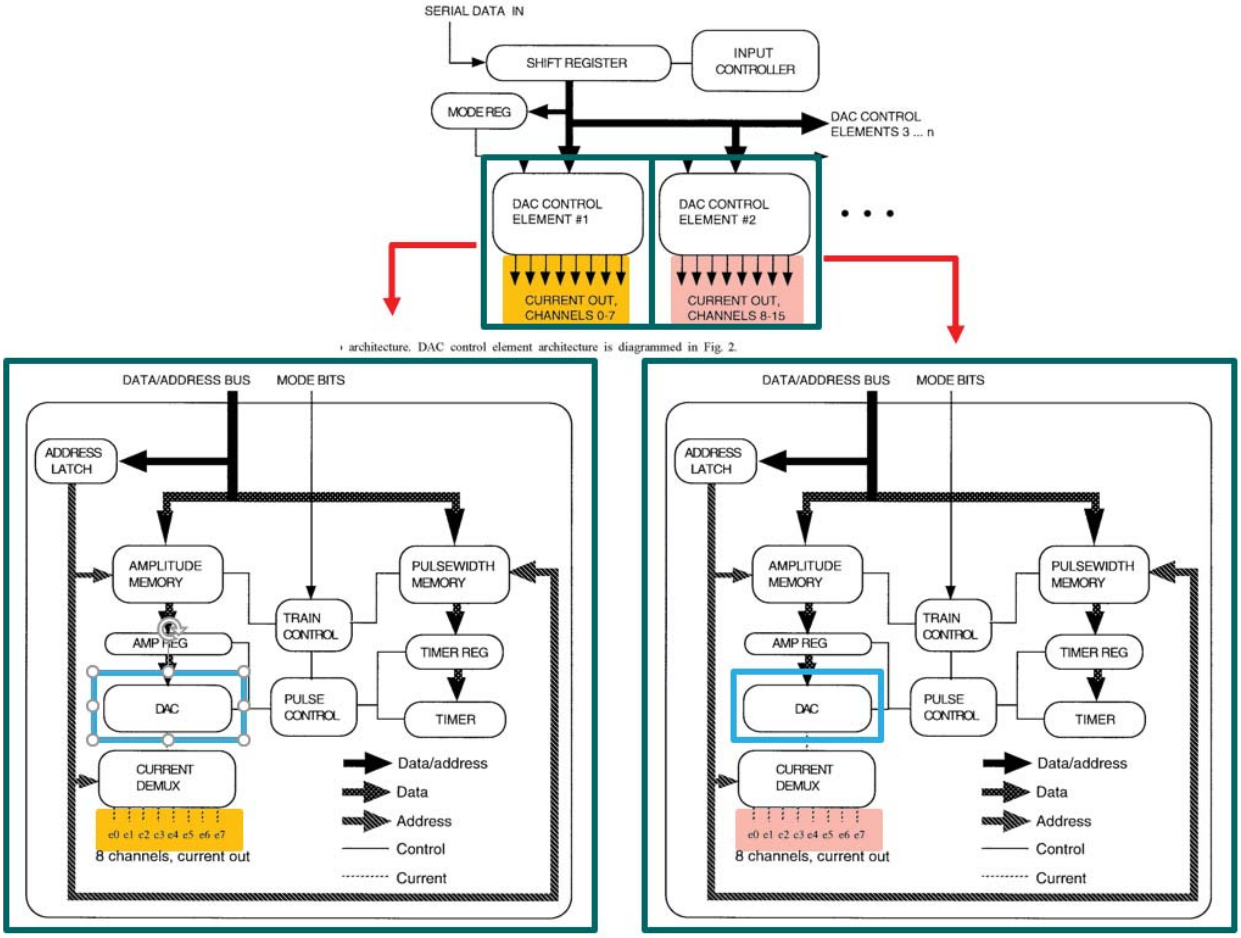
Next, Jones discloses that the next 3 significant bits (*i.e.*, a_4 a_3 a_2) are used to "address one of eight individual channels (electrodes) within a DAC subsystem." Ex. 1006, 1215. In other words, Jones requires multiple electrodes share the same binary values of the following bits: a_4 a_3 a_2. Ex. 1003, ¶217. As explained above, *see* § VI.E.2.iv, the annotated Figures 1 and 2 of Jones shows 2 different DACs and each DAC has its own set of 8 electrodes. Accordingly, electrode pairs—1 from each DAC set—share the same binary values for the 3-channel address lines (*i.e.*, a_4 a_3 a_2). Ex. 1003, ¶217. When a_1 a_0 are set equal to "11" for a "normal message" ($a_6 = 0$), Jones' chip architecture activates one of the 8 given electrode groups illustrated above depending on the remaining address fields. Ex. 1006, Figs. 1-2 (annotated), 1215 (explaining the use of the following address bits: a_6 a_5 a_4 a_3 a_2 a_1 a_0.) Ex. 1003, ¶218.

As shown above, Jones' chip architecture arranges each electrode in one of 8 groups based on an electrodes assigned binary values for the 3-channel address lines: $a_4\, a_3\, a_2$. Ex. 1003, ¶219. Thus, Jones discloses "*L number of electrode contact groups*," where L = 8.

vi. *DAC to Switch Coupling*

Claim 6 also recites *"wherein each DAC (12) of the N number of DACs is coupled to one of the N grouped sets (110) of switches (121)."* Jones discloses this limitation, specifically that N = 2. Ex. 1003, ¶¶220-224.

As shown above, Figure 1 of Jones shows 2 DAC control elements. Ex. 1006, Figs. 1-2, 1213. Each DAC subsystem has a DAC (blue boxes) and "eight channels (electrodes) to be serviced" (orange and pink boxes) shown below:



Ex. 1006, 1213 Figs. 1 and 2 (annotated), Ex. 1003, ¶221.

As shown above, Figure 1 of Jones shows 2 DAC subsystems (*i.e.*, "DAC Control Element #1" and "DAC Control Element #2") that each have a DAC connected to a set of 8 different electrodes via a "Current Demux." Ex. 1003, ¶222.

As explained above, *see* §VI.E.2.iii, the annotated Figure of Jones has 16 CMOS passgates that are switches divided into two different switch groups: an orange switch group and pink switch group. Ex. 1003, ¶223. The annotated

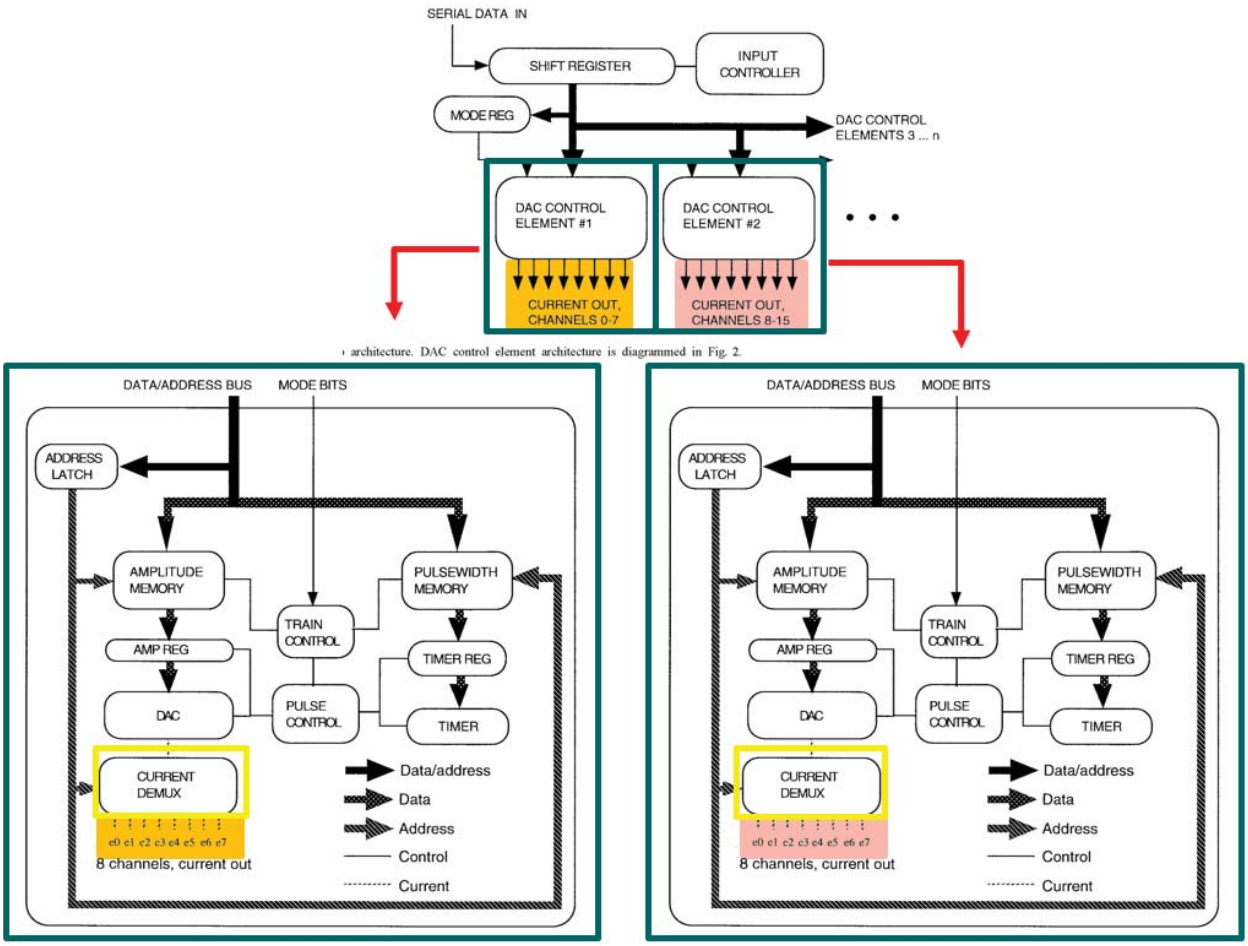
Figure also shows that the DAC from "DAC control element 1" is connected to 8 switches in the orange switch group. Ex. 1003, ¶223. Likewise, the DAC from "DAC control element 2" is connected to 8 switches located in the pink switch group. Ex. 1003, ¶223.

Accordingly, Jones discloses "*each DAC (12) of the N number of DACs is coupled to one of the N grouped sets (110) of switches*."

vii. *Switch to Electrode Contact Coupling*

Claim 6 also recites "*wherein each switch (121) in one of the N set (110) of switches, in turn, is uniquely coupled to only one electrode contact (130) in each of L groups (100) of electrode contacts*." Jones discloses this limitation for N = 2 and L = 8. Ex. 1003, ¶¶225-228.

As explained above, *see* §VI.E.2.iii, Jones provides 2 DAC control elements that each have 8 CMOS passgates ("*switches*") in 2 switch groups (i.e., an orange switch group and pink switch group) shown below:



Ex. 1006, 1213, Figs. 1 and 2 (annotated), Ex. 1003, ¶226.

Jones further discloses that the 8 CMOS passgates ("*switches*") "determine which of the eight channels is active, and also connect all of the unused channels to the exhaust line." Ex. 1006, 1216. Each CMOS passgate is associated with 1 channel and its corresponding electrode. Ex. 1003, ¶227. For both the orange and pink switch groups (each "*one of the N set of switches*"), each CMOS passgate is "*uniquely coupled*" to one of the 8 electrodes associated with that switch group ("*uniquely coupled to only one electrode contact*"). Ex. 1003, ¶227

Each CMOS passgate and corresponding electrode is activated based on the electrode group designated by the 3-channel address lines which thereby defines "*L groups (100) of electrode contacts*." Ex. 1003, ¶228. To determine which channel is active, Jones discloses that the CMOS passgates are "selected by a three-to-eight decoder which decodes the three-channel address lines." Ex. 1006, 1216. As explained above, *see* §VI.E.2.v, the 2 DACs have 8 electrode groups—*i.e.*, 8 groups (L= 8) with 1 electrode from each DAC—that each have their own binary values for the 3-channel address lines (*i.e.*, $a_4\, a_3\, a_2$). Ex. 1003, ¶228. Each CMOS passgate ("*switch*") uses the binary values from 3-channel address lines to determine whether to activate its corresponding electrode. *Id.*; Ex. 1003, ¶228. Accordingly, Jones discloses "*wherein each switch (121)…is uniquely coupled to only one electrode contact (130) in each of L groups (100) of electrode contacts*."

viii. *Wherein Clause*

Claim 6 recites *"wherein the whole numbers N., L and M are chosen such that, NxL=M; wherein M is greater than N."* Jones discloses this limitation. Ex. 1003, ¶¶229-230.

As explained above, *see* §§VI.E.2.ii, VI.E.2.iv, VI.E.2.v, the annotated Figures 1 and 2 of Jones shows 2 DACs (N=2), 16 electrode contacts (M=16), and 8 electrode groups (L= 8). Ex. 1003, ¶230. Accordingly, Figures 1 and 2 of Jones shows a chip architecture with N = 2, M = 16, and L = 8. N, M, and L are thus

"*whole numbers*" and "*NxL=M*" (*i.e.*, 2 x 8 = 16). Ex. 1003, ¶230. Therefore, Jones discloses "*wherein the whole numbers N., L and Mare chosen such that, NxL=M; wherein M is greater than N*."

3. Claims 7 and 8

Claim 7 recites *"[t]he system of claim 6, wherein the switches are transistor switches*" and claim 8 recites *"[t]he system of claim 7, wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors."*

Figure 2 of Jones shows sixteen CMOS passgates, which are "*switches*." A CMOS passgate is a switch made up of transistors. Ex. 1003, ¶232. A CMOS transmission gate "consists of one *n*-channel and one *p*-channel MOS transistors connected in parallel." Ex. 1007, 427. In addition, a CMOS transmission gate is "essentially an electronic switch that is controlled by an input logic level." Ex. 1007, 427. Accordingly, a CMOS transmission gate is a "*transistor switch*." Ex. 1003, ¶232. As Jones' CMOS passgates are CMOS transmission gates, Jones' CMOS passgates are thus "*transistor switches*" made up of "PMOS transistor[s]." Ex. 1003, ¶234; Ex. 1007, 427.

4. Claim 9

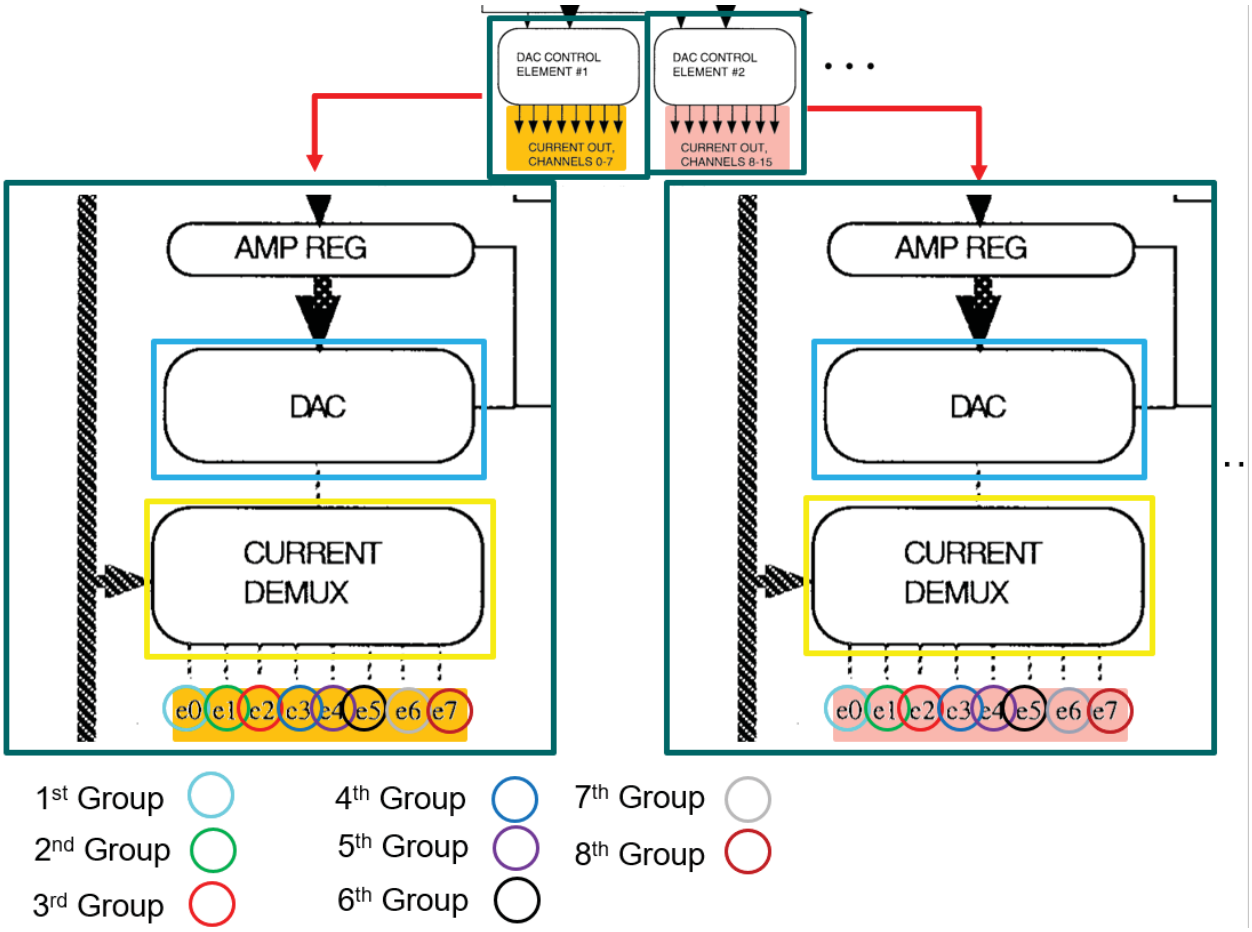
Claim 9 recites *"[t]he system of claim 6, wherein the switches are programmable using software or hardware programming."*

Jones discloses that a user operates the chip by "send[ing] a serial data stream." Ex. 1006, 1211. Once the chip receives the data stream, "[c]ircuitry decodes this serial data stream, and writes the appropriate amplitude byte to the addressed DAC's amplitude register." Ex. 1006, 1211; Ex. 1003, ¶236. Further, the serial data stream includes a "controlled electrode address" that has a 7-bit addressing field. *Id*. These seven addressing bits are "used to access all channels and registers on the chip." Ex. 1006, 1215. Accordingly, because it defines channel access, a user programs the DAC hardware and corresponding electrodes in Jones' chip using a serial data stream. Ex. 1003, ¶236. Hence, Jones discloses that the switches are "*programmable using software or hardware programming*."

5. Claim 10

Claim 10 recites *"[t]he system of claim 9 wherein the programming allows electrode contacts (130) only one electrode contact group (100) or, a subset thereof, among the L contact groups (100) to pass current in a single time duration* T_d*."*

As explained above, *see* §VI.E.2.v, Jones' chip architecture allows each individual electrode group (shown below) to be activated (i.e., closing an electrode's associated CMOS pass-gate) when a_1 a_0 are set equal to "11" for a "normal message" ($a_6 = 0$):



Ex. 1006, Fig. 3 (annotated), 1215 (explaining the use of the following address bits: $a_6\, a_5\, a_4\, a_3\, a_2\, a_1\, a_0$.); Ex. 1003, ¶238. The above activated electrodes belong to "*only one electrode group*" at a time. Ex. 1003, ¶238. Accordingly, Jones discloses that the "*programming allows electrode contacts only one electrode contact group…among the L contact groups.*"

Alternatively, Jones also discloses that Jones' chip architecture may set an address field (i.e., $a_1\, a_0$) to "select an individual DAC on the chip." Ex. 1006, 1215. Jones' address field may be used to select a single electrode from 1 DAC—*i.e.*, one electrode is a "*subset thereof*" of an electrode group. Ex. 1003, ¶239.

Accordingly, Jones' also discloses "*programming allows… a subset thereof, among the L contact groups (100).*"

Jones further discloses that the selected electrodes are stimulated using a "complete[d] biphasic pulse through the DAC." Ex. 1006, 1215. These pulses last for time that is controlled by register T_1. Ex. 1006, 1215. ("It loads the timer with the pulse width (register T_1), turns on the DAC, and awaits a time-out signal from the timer."); Ex. 1003, ¶240. Accordingly, Jones' selected electrode(s) are active for a single time duration that is selected by register T_1 ("*to pass current in a single time duration T_d*"). Ex. 1003, ¶240

6. Claim 15

Claim 15 is disclosed by Jones for the same reasons described above for claim 6. Specifically, Jones discloses "*[a] method of switching outputs in a multi-channel stimulator, said method comprising:*" (§ VI.E.2.i), "*(a) providing N number of DACs (12)*" (§ VI.E.2.ii), "*(b) providing M number of electrode contacts (130) and M number of switches (110)*" (§ VI.E.2.iii), "*(d) coupling each switch (121) within the at least one set (110) of switches, uniquely to one of the M electrode contacts (130)"* (§ VI.E.2.vii), and *"wherein the whole numbers N., L and M are chosen such that M=NXL, and M is greater than N*" (§ VI.E.2.viii). Ex. 1003, ¶¶241-243, 246, 251.

Jones further discloses "*(c) coupling each of N DACs (12) to at least one set (110) of switches having L number of switches (121) in the at least one set (110)"* (§§ VI.E.2.iii, vi). Ex. 1003, ¶244. Jones provides 2 DAC control elements that between them have 16 CMOS passgates, or 8 each ("*L number of switches*"). Ex. 1006, 1213, Figs. 1 and 2, Ex. 1003, ¶244. Jones thus discloses L = 8. As shown above, each of the 2 DACs ("*N DACs*") has its own set of 8 CMOS passgates connected to electrodes in the orange and pink boxes. Ex. 1003, ¶245.

Jones also discloses "*(e) causing current to flow through selected electrode contacts (130) at any one time duration, T_d, by closing the associated switches (121).*" The selected electrodes are stimulated using a "completed biphasic pulse through the DAC." Ex. 1006, 1215. These pulses last for time that is controlled by register T_1. Ex. 1006, 1215. ("It loads the timer with the pulse width (register T_1), turns on the DAC, and awaits a time-out signal from the timer."). As shown above, *see* §VI.E.5, Jones discloses a chip architecture program that selects which CMOS pass-gates to activate thereby stimulating the corresponding electrode. Accordingly, Jones' selected electrode(s) are active for a single time duration that is selected by register T_1 ("*at any one time duration T_d*"). Ex. 1003, ¶248.

At the appropriate time, Jones's system selects which electrode to activate using CMOS passgates. For example, Jones discloses that the "Current Demux" is a "set of eight CMOS passgates, selected by a three-to-eight decoder…" Ex. 1006, 1216.

Jones' CMOS passgates are "*switches*." Ex. 1003, ¶249. "The passgates determine which of the eight channels is active, and also connect all of the unused channels to the exhaust line." Ex. 1006, 1216. When a channel is activated by "*closing the associated switch[]*" current will *"flow through the selected electrode contact[]."* Ex. 1003, ¶249.

7. Claims 16 and 17

Claim 16 recites *"[t]he method of claim 15 wherein the Switches are transistor Switches*" and claim 17 recites *"[t]he method of claim 16 wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors."* Jones discloses these limitations for the same reasons provided for claims 7 and 8. Ex. 1003, ¶¶252-253.

8. Claim 18

Claim 18 recites *"[t]he method of claim 15 wherein the Switches are Software programmable."* Jones discloses this limitation for the same reasons provided for claim 9. Ex. 1003, ¶254.

9. Claim 19

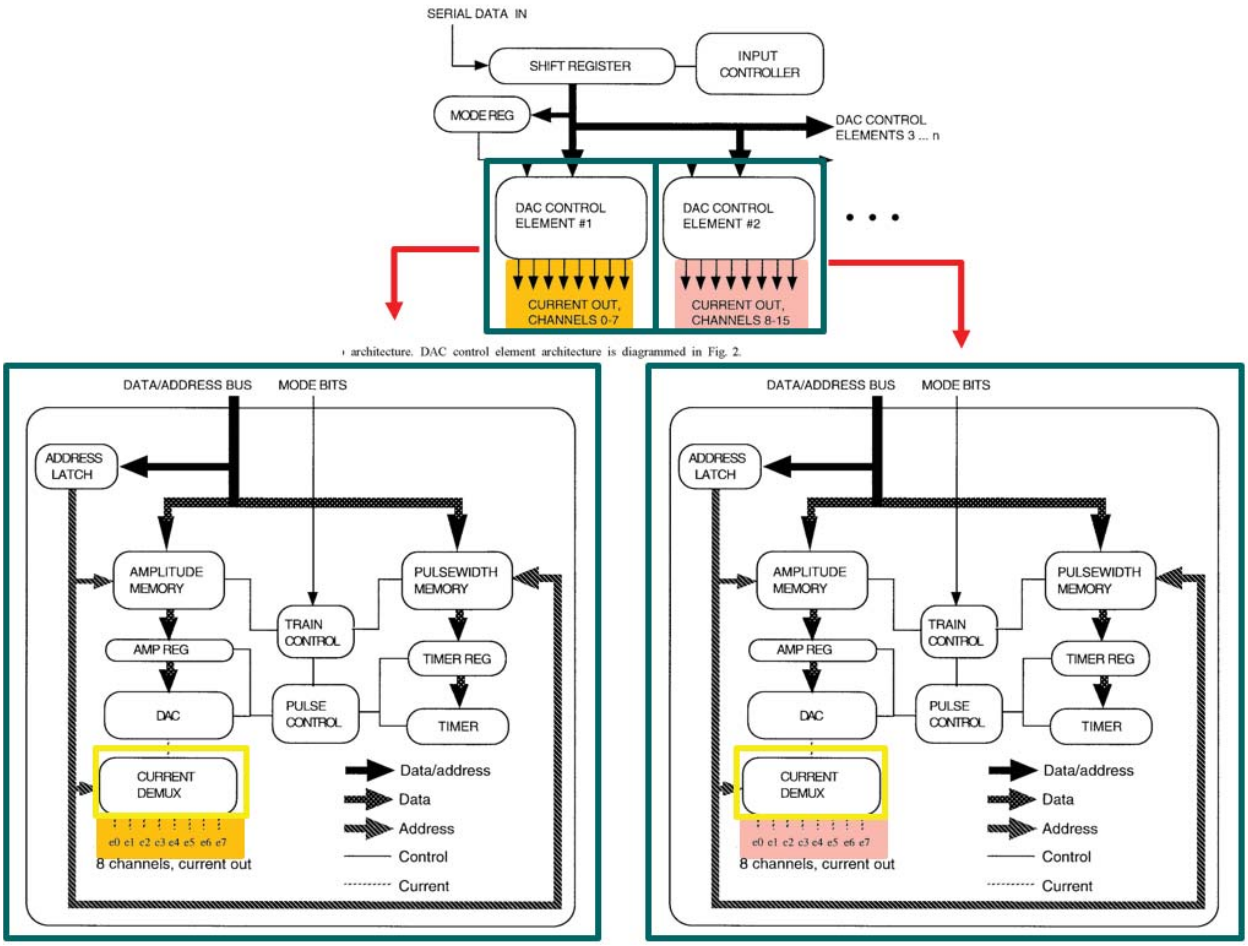
Claim 19 recites *"[t]he method of claim 15 wherein the step (e) of causing current to flow through a selected group of electrode contacts is accomplished by causing current to flow in only one of L number of electrode contact groups (100)*

at any one time duration, T_d." Jones discloses this limitation for the same reasons provided for claim 10 and limitation [e] of claim 15. Ex. 1003, ¶255.

F. Claims 6-10 and 15-19 Are Obvious Over Jones (Ex. 1006)

1. "Each Switch … Is Uniquely Coupled to Each Electrode"

Claims 6 and 15 require that "*each switch (121) in one of the N set (110) of switches, in turn, is uniquely coupled to only one electrode contact (130) in each of L groups (100) of electrode contacts*" and "*each of the M switches (31) uniquely to each of M electrode contacts (31)*," respectively. As discussed above (§ VI.E.2.vii), Jones discloses 2 DAC control elements that each have 8 CMOS passgates ("*switches*") in 2 switch groups (i.e., an orange switch group and pink switch group) shown below:



To the extent that Patent Owner argues that Jones does not disclose that "*each switch … is uniquely coupled to only one electrode contact*," it would have been obvious to modify the disclosed system to have such a unique coupling. As explained above (§ VI.E.2.v), there are equally as many switches as electrodes in the system disclosed by Jones, and each electrode has a binary value. Ex. 1003, ¶257. It was well-known to implement de-multiplexers with a single switch per output, with control signals selecting which switch would pass through the input. *E.g.*, Ex. 1011, p. 474 (Fig. 5); Ex. 1013, p. 3 (Figure labeled CD4051BC). This

allows for arbitrarily wide de-multiplexing by simply adding more switches. *Id.*; Ex. 1003, ¶257. It would have been obvious to one of ordinary skill to implement the design such that the switches and electrodes have a 1-to-1 arrangement because it is the simplest and easiest to implement solution that satisfies the requirements of the remainder of the system. Ex. 1003, ¶258. One of ordinary skill would not have applied a more complicated arrangement in the system disclosed by Jones when the simpler 1-to-1 arrangement meets the needs of the system. *Id*. Moreover, independent coupling isolates the electrodes and prevents failures in 1 switch-electrode pair from affecting the functionality of the other switch-electrode pairs. Ex. 1003, ¶259.

2. "Electrode Contact Groups"

Claim 6 requires "*L number of electrode contract groups*." To the extent that Patent Owner argues that Jones does not expressly disclose "*electrode contact groups*," such a feature would have been obvious.

As explained above, *see* §VI.E.2.v, electrode pairs—1 from each DAC set—share the same binary values for the 3-channel address lines (*i.e.*, $a_4\, a_3\, a_2$). A POSA would have found it obvious to use these address lines to stimulate 2 electrodes from different DACs simultaneously. Ex. 1003, ¶261. A POSA would further have recognized that it could send a single message to both DACs to operate electrodes sharing the same address line, such as electrode 3 from both

DACs. Ex. 1003, ¶261. In doing so, a POSA would have recognized that sending a single message instead of 2 separate messages reduces the throughput on Jones' system. Ex. 1003, ¶261. Hence, it would have been obvious to use 1 message that groups the electrodes with the same binary values for their address lines to simultaneously stimulate the group. Ex. 1003, ¶261.

G. Claims 7, 8, 16, and 17 are rendered obvious by Jones (Ex. 1006) in view of Panescu (Ex. 1008)

Claims 7 and 16 recite "*wherein the switches are transistor switches*" Claims 8 and 17 depend on claims 7 and 16, respectively, and further recite "*wherein the transistor switches are selected from the group consisting of PMOS or MOS transistors.*"

To the extent that Patent owner argues that the Jones' switches are not "*transistor switches*" that are "*selected from a group consisting of PMOS or MOS transistors*," it would have been obvious to use Panescu's PMOS-based switches in Jones' system. Panescu is analogous art as justified above. *See* §VI.C. Likewise, Jones is analogous art to the '298 patent because it also is in the field of electrode stimulation. Ex. 1001, 1:11-14; Ex. 1006, 1210; Ex. 1003, ¶264.

As shown above, *see* §VI.C, Panescu discloses "*transistor switches*" that are "*are selected from the group consisting of PMOS or MOS transistors*." Moreover, PMOS and MOS transistors were well-known electrical components used for electrical switches as shown above. *See* §VI.C. Hence, it would have been

obvious to use Panescu's switches made up of PMOS transistors for Jones' switches. Ex. 1003, ¶265. This would have been simply an arrangement old elements (*i.e.*, switches made up of PMOS transistors) with each performing the same function it had been known to perform (*i.e.*, electronic switching) and yielded no more than one would expect from such an arrangement. Ex. 1003, ¶265. Therefore, it would have been obvious. *KSR Intl Co.*, 550 U.S. at 417.

H. No Secondary Considerations Exist

Nevro is unaware of any assertion by BSNC that secondary indicia of non-obviousness exist having a nexus to any invention of the '298 patent, but reserves its right to respond to any such subsequent assertion.

VII. CONCLUSION

For the foregoing reasons, the challenged claims are unpatentable.

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EXHIBIT LIST

No.	Exhibit Description
1001	U.S. Patent No. 7,127,298 ("298 Patent")
1002	File History of U.S. Patent No. 7,127,298 ("298 File History")
1003	Declaration of Benjamin Pless
1004	Curriculum Vitae of Benjamin Pless ("Pless-CV")
1005	Hitzelberger et al., *A Microcontroller Embedded ASIC for an Implantable Electro-Neural Stimulator*, Proceedings of the 27th European Solid-State Circuits Conference, 428-431 (Frontier Group 2001) ("Hitzelberger") (as included on Conference CD)
1006	K. Jones and R. Normann, *An Advanced Demultiplexing System for Physiological Stimulation,* IEEE Transactions on Biomedical Engineering, Vol. 44, No. 12, pp. 1210-1220 (1997) ("Jones")
1007	M. Mano, "Digital Integrated Circuits," *Digital Design*, pp. 398-433 (Prentice Hall 3 ed. 2002).
1008	U.S. Patent No. 6,101,410 to Panescu et al. ("Panescu")
1009	U.S. Patent No. 6,219,580 to Faltys et al. ("Faltys")
1010	*Boston Scientific Corp. et al. v. Nevro Corp.*, Case No. 1-18-cv-00644 (D. Del.)
1011	Datasheet for CD4051BC, CD4052BC, and CD04053BC, *Fairchild Semiconductor* (Nov. 1983 revised August 2000)
1012	U.S. Patent No. 6,181,969 to Gord ("Gord")
1013	T. R. Gheewala et al., *A CMOS Implantable Multielectrode Auditory Stimulator for the Deaf*, IEEE Journal of Solid-State Circuits, Vol. SC-10, No. 6, pp. 472-479 (December 1975)
1014	G. Suaning and N. Lovell, *CMOS Neurostimulation ASIC with 100 Channels, Scaleable Output, and Bidirectional Radio-Frequency Telemetry*, IEEE Transactions on Biomedical Engineering, Vol. 48, No. 2, pp. 248-260 (February 2001)
1015	Declaration of Dr.-Ing. Yiannos Manoli ("Manoli Declaration")
1016	List of Papers by Number, included on CD-ROM distributed at 27th European Solid-State Circuits Conference, September 18-20, 2001
1017	Start page ("default.htm") from CD-ROM distributed at 27th European Solid-State Circuits Conference, September 18-20, 2001
1018	ESSCIRC 2001 conference program: 27th European Solid-State Circuits Conference (September 18-20, 2001), Villach, Austria.

1019	Dr. Manoli's print copy of Hitzelberger et al., *A Microcontroller Embedded ASIC for an Implantable Electro-Neural Stimulator*, Proceedings of the 27th European Solid-State Circuits Conference, 428-431 (Frontier Group 2001)
1020	Library copy of Hitzelberger et al., Hitzelberger et al., *A Microcontroller Embedded ASIC for an Implantable Electro-Neural Stimulator*, Proceedings of the 27th European Solid-State Circuits Conference (Frontier Group 2001)
1021	IEEE Explore Summary of K. Jones and R. Normann, "An advanced demultiplexing system for physiological stimulation," IEEE Journals & Magazine (Abstract), https://ieeexplore.ieee.org/document/649992
1022	IEEE Explore copy of K. Jones and R. Normann, "An Advanced Demultiplexing System for Physiological Stimulation," IEEE Transactions on Biomedical Engineering 44(12): 1210-1220 (1997).
1023	J-C. Voghell, et al., *Programmable Current Source Dedicated to Implantable Microstimulators*, Proceedings of the Tenth International Conference on Microelectronics, pp. 67-70 (1998)

CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,988 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I hereby certify that on this 18th day of July, 2019, I caused to be served a true and correct copy of the foregoing and any accompanying exhibits by Federal Express on the following counsel:

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