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Paper 14
Entered: November 23, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

JOHNSON & JOHNSON SURGICAL VISION, INC.,
Petitioner,

v.

ALCON INC.,
Patent Owner.

IPR2021-01003
Patent 8,398,236 B2

Before MIRIAM L. QUINN, CHRISTOPHER M. KAISER, and JAMIE T. WISZ, *Administrative Patent Judges*.

QUINN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Johnson & Johnson Surgical Vision, Inc. ("Petitioner") filed a Petition (Paper 2, "Petition" or "Pet.") requesting an *inter partes* review of claims 1–3, 6–13, 15–19, 21, 23, 26–32, 34–38, and 40 ("the challenged claims") of U.S. Patent No. 8,398,236 B2 (Ex. 1001, "the '236 patent") pursuant to 35 U.S.C. §§ 311–319. Alcon Inc. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Preliminary Response" or "Prelim. Resp.").

The standard for institution is set forth in 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows that "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314 (2018); *see also* 37 C.F.R § 42.4(a) ("The Board institutes the trial on behalf of the Director."). Upon consideration of the parties' contentions and the evidence of record, we conclude that Petitioner has not established a reasonable likelihood of prevailing in demonstrating the unpatentability of at least one challenged claim of the '236 patent. Accordingly, we deny Petitioner's request and do not institute an *inter partes* review.

II. BACKGROUND

A. Real Parties in Interest

Petitioner indicates that the real parties-in-interest include Johnson & Johnson Surgical Vision, Inc., and its subsidiaries AMO Development, LLC, AMO Manufacturing USA, LLC, and AMO Sales and Service, Inc. Pet. 67.

Patent Owner indicates that its real parties-in-interest include Alcon Inc., Alcon Vision, LLC, and Alcon Research, LLC. Paper 5.

B. The '236 Patent

The '236 patent "relates to systems and methods for docking ophthalmic surgical systems to a surgical eye with high precision." Ex. 1001, 1:8–10. According to the '236 patent, "[m]any ophthalmic surgical systems include a docking unit, or patient interface, that makes contact with a surgical eye and keeps it effectively immobile relative to an objective of the surgical system during an ophthalmic procedure." *Id.* at 4:59–62. "The precision of the ophthalmic procedure can be increased by increasing the precision of the alignment of the docking unit with the target of the surgery." *Id.* at 4:62–65. However, certain surgeries pose "challenges for the alignment and docking of the patient interface for several reasons." *Id.* at 5:3–5. These include a target lens located inside the eye that is less visible to the surgeon, patients having difficulties following instructions by the surgeon during the alignment process, target lens that are displaced and tilted within the eye, and pressure from the docking unit that displaces the lens. *Id.* at 5:5–22. The '236 patent purports to solve these problems by providing "docking procedures" using imaging techniques. *Id.* at 5:23–26.

The '236 patent states that some systems use a second imaging system such as an "optical coherence tomography (OCT) imaging system" that includes an OCT imaging unit. *Id.* at 6:30–35. The OCT imaging unit "creates an OCT imaging beam, guides the OCT imaging beam toward the eye and processes the OCT imaging beam returned from the eye." *Id.* at 6:35–37. The OCT imaging system "can also include an OCT x-y scanner" that scans the OCT imaging beam across the target region in the x-y plane. *Id.* at 6:37–40.

Figure 10 illustrates an image-guided docking system of the '236 patent and is reproduced below.

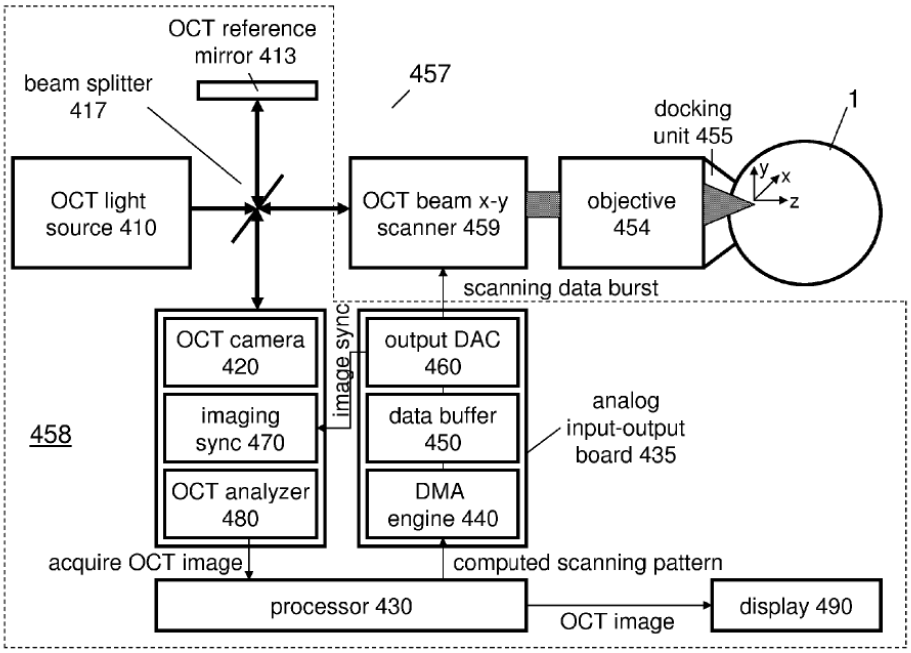

FIG. 10

Figure 10 shows OCT imaging system 457 having OCT imaging unit 458 and OCT x-y scanner 459. *Id.* at 11:38–41. According to the '236 patent, OCT light source 410 produces an OCT imaging beam guided by OCT x-y scanner 459, and directed to the eye via objective 454 and docking unit 455. *Id.* at 11:45–47, 12:3–5. OCT x-y scanner 459 scans the OCT imaging beam in the eye in the x and y directions. *Id.* at 12:5–9. The OCT imaging beam that is returned from the eye is unified with the reference beam returning from OCT reference mirror 413 at beam splitter 417, and carries the imaging information that is recorded by OCT camera 420. *Id.* at 12:13–17. OCT analyzer 480 processes the image data using a Fast Fourier Transform (FFT), which "converts the interference information of different wavelength components into image information corresponding to different z-depths." *Id.* at 12:37–41. The transformed OCT image data is then forwarded to processor 430, which generates an OCT image and outputs the generated OCT image towards display 490. *Id.* at 12:41–46.

The ’236 patent states that, however, there are “difficulties [in] the operation of some existing OCT scanning-beam-controllers.” *Id.* at 12:47–50. In some OCT imaging systems where processor 430 can multitask, the processor performs an “interrupt” by switching from the task of scanning the beam to another task, which results in a “scanning-freeze” that “disrupt[s] the timing of the x-y scan, introducing an error and noise into the coordinates of the imaged location.” *Id.* at 12:51–61. According to the ’236 patent, “[t]his timing error in the outputted scanning data can lead to delays that may reach 50, 100 or more microseconds: a phenomenon sometimes called jitter.” *Id.* at 12:61–63.

The ’236 patent, therefore, provides analog input-output board 435 that includes a local or dedicated memory controller, also referred to as a direct memory access engine (DMA engine) 440, data buffer 450, and output digital-analog converter (DAC) 460. *Id.* at 13:30–42. DMA engine/memory controller 440 manages the transfer of the computed scanning data, indirectly or directly, from processor 430 toward data buffer 450. *Id.* at 13:32–38. And data buffer 450, coupled to local memory controller 440, stores the scanning data and outputs the scanning data towards output DAC 460. *Id.* at 13:32–38. Output DAC 460 is coupled to data buffer 450 and (i) converts selected outputted scanning data to analog scanning signals, and (ii) outputs the scanning signals towards OCT scanner 459. *Id.* at 13:38–42.

Further, the OCT scanning beam-controller can be implemented by having the dedicated DMA engine transfer the scanning data from a processor memory to a data buffer that is a first-in-first-out (FIFO) memory. *Id.* at 13:45–51. The FIFO buffer memory, when prompted, outputs the stored scanning data without sending the scanning data through the shared bus. *Id.* at 13:51–56. According to the ’236 patent, in some

implementations, the speed of the output of the output DAC "can be so fast" that an operating speed of imaging system 457 is limited by an integration time of OCT camera 420. *Id.* at 15:1–4.

C. Related Matters

The parties indicate that the '236 patent is the subject of the following district court litigation: AMO Development, LLC v. Alcon LenSx, Inc, No. 1:20-cv-00842-CFC (D. Del.). Pet. 67; Paper 5.

D. Illustrative Claim

Of the challenged claims, claims 1, 27, and 35 are independent. Claims 27 (an apparatus claim) and 35 (a method claim) appear to be broader in scope than claim 1 (a further method claim), because those claims do not require aligning and realigning a docking unit. For ease of reference, we reproduce below claim 27, as representative of the claimed subject matter.

> Claim 27. An imaging controller for an ophthalmic system, comprising:
>
> a processor that computes scanning data for a scanning pattern of an optical coherence tomographic imaging system;
>
> a local memory controller that partially manages a transfer of the computer scanning data from the processor to a dedicated data buffer, wherein
>
> the dedicated data buffer is configured to store the scanning data and to output the scanning data; and
>
> an output digital-analog converter, coupled to the dedicated data buffer that converts selected scanning data to analog scanning signals and outputs the scanning signals to the optical coherence tomographic imaging system.

Ex. 1001, 19:45–60.

E. Asserted Grounds and Testimony

Petitioner asserts the following grounds.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
27–32, 35–38, 40	103	Ustun,[1] LabVIEW Help,[2] Breyer[3]
35–38, 40	103	Ustun, LabVIEW Help, Breyer, RIO Manual[4]
34	103	Ustun, LabVIEW Help, Bryer, Hammer[5]
1–3, 6, 7, 9–13, 15, 18, 19, 21, 23, 26	103	Culbertson,[6] Ustun, LabVIEW Help, Breyer

[1] Teoman E. Ustun, et al., *Real-time processing for Fourier domain optical coherence tomography using a field programmable gate array,* 79 Review of Scientific Instruments, 114301, 1–10 (2008), filed as Exhibit 1008 ("Ustun").

[2] National Instruments Webpage, *Transferring Data Between the FPGA and the Host VI (FPGA Module),* LabVIEW FPGA Module 8.5 Help, produced from web.archive.org, filed as Exhibit 1007 ("LabVIEW Help").

[3] U.S. Patent Pub. No. 2007/0088865 A1, published April 19, 2007, filed as Exhibit 1005 ("Breyer").

[4] National Instruments, *Reconfigurable I/O, NI 783 xR User Manual*, filed as Exhibit 1006 ("RIO Manual").

[5] Daniel Hammer, et al., *Three-dimensional tracker for spectral domain optical coherence tomography,* 6429 Proceedings of SPIE 642913, 1–10 (2007), filed as Exhibit 1009 ("Hammer").

[6] U.S. Patent Pub. No. 2009/0012507 A1, published January 8, 2009, filed as Exhibit 1010 ("Culbertson").

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
8	103	Culbertson, Ustun, LabVIEW Help, Breyer, Kankaria[7]
16, 17	103	Culbertson, Ustun, LabVIEW Help, Breyer, Hammer

Petitioner also presents testimony from Dr. Robert Huber, in support of its Petition. Ex. 1003 ("Huber Decl."). Patent Owner presents testimony of Dr. Omid Kia, in support of its Preliminary Response. Ex. 2001 ("Kia Decl.").

III. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner proffers a level of ordinary skill in the art that sets the minimum standard at having a Bachelor's degree in electrical engineering, computer science, or a related field, and three to four years of industry experience. Pet. 8. Patent Owner agrees that a degree in electrical engineering is necessary and adds that a person of ordinary skill in the art must understand the electronic components at issue. Prelim. Resp. 17. Patent Owner further remarks that Petitioner's declarant, Dr. Huber, lacks the qualifications to meet the proffered level of ordinary skill in the art because Dr. Huber lacks the proposed bachelor's degree. *Id.* Patent Owner further remarks that Dr. Kia, on the other hand, satisfies the proffered level of ordinary skill in the art because Dr. Kia has a Ph.D. in electrical engineering and has the requisite work experience. *Id.*

[7] Manish Kankaria, *Design and construction of a fast spectrometer for Fourier domain optical coherence tomography,* Doctoral Thesis, University of Texas at Arlington, May 2006, filed as Exhibit 1011 ("Kankaria").

For our analysis on whether to institute, we need not determine the level of ordinary skill in the art or whether any of the declarants satisfies such a level. Neither party argues that the obviousness determination hinges on the level of ordinary skill. Accordingly, we do not find it necessary to define the level of skill with specificity save to note that the level of ordinary skill is evidenced by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (stating that the absence of specific findings on the level of skill in the art does not give rise to reversible error where the prior art itself reflects an appropriate level and a need for testimony is not shown).

B. Claim Construction

In *inter partes* review proceedings based on petitions filed on or after November 13, 2018, such as this one, we construe claims using the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* 37 C.F.R. § 42.100(b).

Petitioner asserts that all terms should be given their ordinary and customary meaning, without pointing out any particular construction for significant terms in the claim. Pet. 9. Patent Owner points out that the parties submitted claim construction positions in district court and that Petitioner's position on a disputed term appears to be inconsistent with that position. Prelim. Resp. 27–28 (pointing to Exhibit 1008). We need not determine preliminarily the construction for any claim term as our decision does not rely on any.

C. Obviousness Grounds

Having reviewed the Petition and the arguments and evidence in opposition we determine that Petitioner has not shown a reasonable

likelihood of prevailing on its assertion that the challenged claims are unpatentable under the asserted grounds. We begin with a brief explanation of Ustun.

1. Overview of Ustun (Ex. 1008)

Ustun relates to "[r]eal-time display of processed Fourier domain optical coherence tomography (FDOCT) images" that "is important for applications that require instant feedback of image information, for example, systems developed for rapid screening or image-guided surgery." Ex. 1008, 1, Abstr. Ustun indicates that "the computational requirements for high-speed FDOCT image processing usually exceeds the capabilities of most computers." *Id.* Ustun purports to solve this problem by developing an image processing system having "a field programmable gated array, firmware, and software that enables real-time display of processed images at rapid line rates." *Id.* Ustun's system is flexible such that it can be "inserted in-line between any FDOCT detector and any Camera Link frame grabber." *Id.*

Ustun indicates that in ophthalmology, "it is desirable to have real-time feedback to aid in patient alignment and reduce session time." *Id.* at 2. To provide "rapid processing and real-time display of FDOCT images," Ustun develops "digital signal processing (DSP) hardware using a single field programmable gate array (FPGA) integrated circuit (IC) and a custom electronics board." *Id.* Ustun's firmware provides "full implementation of the FDOCT signal processing chain inside the FPGA IC." *Id.*

Figure 1(a) of Ustun is reproduced below.

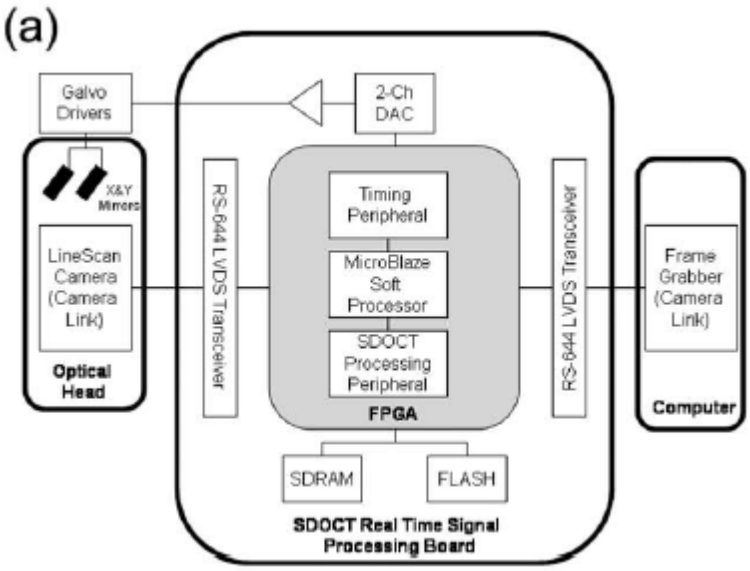

Figure 1(a) is a schematic of Ustun's "real-time spectrometer-based FDOCT DSP hardware." *Id.* at 3. The DSP hardware "consists of an off-the-shelf FPGA minimodule (Avnet Inc.) that plugs into a custom electronics board." *Id.* "The central component of the design is a high-performance FPGA with a fully parallel architecture, around which all other elements are integrated." *Id.* Ustun discloses that its "FPGA has 1536 configurable logic blocks (CLBs) that are the main logic resource for implementing sequential and combinatorial circuits." *Id.* Tasks performed inside the FPGA include transferring "either raw or processed FDOCT image data to the computer," controlling and synchronizing "all external hardware components," driving "the digital-to-analog converter (DAC) IC," and coordinating "the low-speed data transfer to and from the computer over the internal Camera Link RS-232 serial port." *Id.* Ustun further discloses that its FDOCT processing peripheral "is connected at its input to the linear array detector over a standard Camera Link interface" and a "standard low voltage digital signal Camera Link receiver IC is used to convert the differential, serial data to a single-ended, parallel format." *Id.* at 3–4.

According to Ustun, a soft processor, the MICROBLAZE processor, "is basically used as a bridge between the computer and the external hardware and custom FPGA peripherals." *Id*. at 4. "The processor is connected to these custom peripherals using the fast simplex link bus, a unidirectional point-to-point communication channel bus." *Id.* Ustun further states that "[p]latform studio integrated development environment and embedded development kit embedded design flow software tools (Xilinx Inc.) were used to develop code for the MICROBLAZE processor." *Id.* Received data "are then relayed to the FDOCT or timing peripheral," and besides handshaking and confirmation packages sent back to the computer, "communication is unidirectional from the computer to the FPGA." *Id.*

In the FDOCT signal processing chain, "first-in, first-out (FIFO) memory buffer is used to capture the incoming data from the detector." *Id.* at 5. To reorganize the interpolation data into an index array and a fixed-point interpolation coefficient array, Ustun utilizes "three BlockRAM memory locations inside the FPGA." *Id.* For data transfer, Ustun discloses that "[a]fter the complete FDOCT signal processing sequence is executed, the axial depth profile is loaded into output FIFO memory" and "[t]his memory functions as a buffer between the FPGA hardware and the computer frame grabber." *Id.* at 6. "The host processor software and graphical user interface were developed with LABVIEW (National Instruments, Inc.) running some MATLAB (Mathworks Inc.) scripts." *Id.* Ustun further discloses that "[t]he primary task of the host processor software is to transfer the FDOCT images frame by frame from the frame grabber memory over the PCI Express bus to the computer internal memory for display on the monitor at the set frame rate with no significant delays." *Id.*

Ustun also discloses that during the initialization process, a user selects certain imaging parameters that are converted to base parameters, such as integration time, and which are "passed to the FPGA to set up camera and galvanometer timing and control signals." *Id.* "The *x-y* galvanometer waveform array is calculated in the host processor software during initialization and downloaded to the FPGA BlockRAM memory and output to the galvanometers via the DAC IC." *Id.* at 7.

2. Reasonable Likelihood Determination – Independent Claims 1, 27, and 35 and Dependents

All challenged independent claims require a "dedicated data buffer." For instance, claim 27 recites transfer of "computed scanning data from the processor to a *dedicated data buffer*, wherein the *dedicated data buffer* is configured to store the scanning data and to output the scanning data." Ex. 1001, 19:52–55 (emphasis added). Claim 35 recites transferring the "scanning control data from the *dedicated data buffer* to a signal converter through a dedicated channel." *Id.* at 20:41–43 (emphasis added). And claim 1 recites "transferring the scanning data by the *dedicated data buffer* to an output module partially under the control of a dedicated memory controller." *Id.* at 17:13–15 (emphasis added). From the plain reading of these claims, we understand that the dedicated data buffer receives scanning data from the processor, and holds that data until it is transferred to an output module (or signal converter).

Petitioner alleges that Ustun's "BlockRAM memory is a dedicated data buffer," because it receives the x-y galvanometer waveform array (i.e., "scanning data") from the host processor. Pet. 22 (citing Huber Decl. ¶ 62). Petitioner posits that "Ustun's BlockRAM is a FIFO buffer because it is

used to temporarily store scanning data before it is 'output to the galvanometers via the DAC IC,'" the DAC IC being the "output module" or "signal converter" required by the claims. *Id.* at n.9 (citing Huber Decl. ¶ 62; Ustun at 7); *id.* at 23 (stating that "Ustun specifically indicates that the scanning data is downloaded to BlockRAM memory (a FIFO buffer)").

Petitioner also argues that a person of ordinary skill in the art would have understood that Ustun's "buffer is to be implemented as a DMA FIFO—a FIFO buffer partially under the control of a DMA engine." Pet. 22 (citing Huber Decl. ¶ 63). Petitioner relies on LabVIEW Help and Breyer to argue that it was known to configure Ustun's BlockRAM as a DMA FIFO buffer. *Id.* at 22–23. And that a person of ordinary skill in the art would have been motivated *to implement* in Ustun a DMA FIFO buffer under the control of a DMA engine. *Id.* at 23.

Patent Owner argues that Ustun does not teach a dedicated data buffer and that it would not have been obvious for Ustun to implement one in its design. In particular, Patent Owner contends that Ustun's BlockRAM is not a buffer, much less a FIFO buffer, and that the reasons Petitioner proffers for implementing a DMA-controlled FIFO buffer in Ustun are deficient. PO Resp. 26–32, 36–42. We agree with Patent Owner's contentions.

a) Petitioner Fails to Show That Ustun's BlockRAM is a FIFO Buffer

As to Petitioner's assertion that Ustun's BlockRAM is a FIFO buffer, we find the record insufficient and Petitioner's evidence lacking. Ustun does not teach or suggest that the BlockRAM is a buffer or a FIFO buffer, and Petitioner has not explained how a random access memory (RAM) would behave as a buffer in Ustun's design. The disclosure of one memory configuration, in this case a RAM, is not a disclosure (or a teaching) of a

buffer, a different memory configuration. Patent Owner's declarant, Dr. Kia, explains that the BlockRAM in Ustun is random access memory configured to work with Ustun's Microblaze processor and it is not a FIFO. Kia Decl. ¶ 73. Dr. Kia explains, and we agree, that Ustun supports this conclusion from the manner in which Ustun describes the initialization process and the real-time display using the initialization data repeatedly. *Id.* ¶¶ 75–76. For instance, it is clear from Ustun's reading and Dr. Kia's explanation that Ustun stores the x-y galvanometer waveform array in the BlockRAM once, at initialization, and that afterwards the repeated real-time display uses the same array already stored. *Id.* (citing Ustun 5, 7–8). Thus, the BlockRAM stores the initialization data during various read cycles, which would not happen if the BlockRAM were a FIFO buffer as Petitioner alleges. *Id.* Indeed, if Ustun had a FIFO buffer, the initialization data would need to be repeatedly downloaded because a FIFO buffer would not retain the stored data once read. *Id.*

These explanations of Ustun's operation successfully rebut the conclusory and factually unsupported allegation in the Petition that "Ustun specifically indicates that the scanning data is downloaded *to BlockRAM memory (a FIFO buffer)*." *See* Pet. 23 (citing Ustun at 7—but Ustun does not describe its BlockRAM as a FIFO buffer) (emphasis added). Additionally, these explanations by Dr. Kia and supported by Ustun's operation show that even if a BlockRAM *could* have been configured to work as a FIFO buffer, there is no teaching or suggestion that Ustun's BlockRAM was indeed implemented as a FIFO buffer. *See* Pet. 23 (arguing that a person of ordinary skill in the art would have known that with LabVIEW, a DMA FIFO could be implemented in the BlockRAM, citing

Exhibit 1018). Consequently, we are persuaded that Ustun's BlockRAM is not a FIFO buffer as Petitioner argues.

Because Petitioner relies on this faulty premise to argue the implementation, in Ustun, of a DMA-controlled FIFO buffer, this issue alone is dispositive of our determination concerning institution. However, giving Petitioner the benefit of the doubt, that it may have relied on either LabVIEW Help or Breyer to contribute the teaching of using Ustun's BlockRAM as a FIFO buffer, we turn now to the discussion of whether it would have been obvious to modify Ustun as alleged.

b) Proffered Motivations to Combine are Deficient

As to Petitioner's assertion that Ustun's BlockRAM "is to be implemented" as a DMA FIFO, we find the proffered reasons to do so insufficient and unsupported by the record. Petitioner argues several reasons to combine the teachings of Ustun's BlockRAM with those of LabVIEW and Breyer. First, Petitioner argues that the "combination is merely an arrangement of old elements to perform the same functions they were known to perform." Pet. 16. This rationale is unpersuasive because it focuses on whether Ustun could have been programmed using either the LabVIEW or Simulink software, not whether Ustun's BlockRAM would have been implemented as a FIFO buffer, or a DMA-controlled FIFO buffer. *See also* Pet. 24 (arguing that a person of ordinary skill in the art "was thus well-equipped to implement the claimed, commonplace, DMA-controlled functionality based on Breyer's teachings, either in LabVIEW or in other graphical programming environments such as Simulink."). The question is not whether Ustun could have been configured to use a different memory scheme, but, rather, whether a person of ordinary skill in the art would have configured Ustun's BlockRAM as alleged. *Belden Inc. v. Berk-Tek LLC*,

805 F.3d 1064, 1073 (Fed. Cir. 2015) ("obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention"); *see also* PO Resp. 37 (arguing that generalized instructions on the use of LabVIEW programming tools, the help manual, and the existence of DMA FIFO technology do not show that a person of ordinary skill in the art would have known the particular application needed to achieve the claimed invention).

Second, Petitioner argues that a person of ordinary skill in the art would have implemented a DMA-controlled FIFO in Ustun because it would significantly improve data speeds. Pet. 17. But as Patent Owner points out, Ustun's design specifically addresses the speed of the data transfer as "sufficient." PO Resp. 38 (citing Ustun at 5). Dr. Kia explains that Ustun intentionally chose to make the transfer "low speed" because it was more than sufficient. Kia Decl. ¶ 94. In contrast, Dr. Huber states that a DMA FIFO configuration was particularly appropriate for transferring large amounts of data, "such as the scanning data for OCT in Ustun." Huber Decl. ¶ 64. This explanation is insufficient because Ustun does not describe the size of its transferred data, such that a person of ordinary skill in the art would recognize that higher speeds would be desirable. The lack of detail in Dr. Huber's testimony, in comparison with the detailed explanations provided by Dr. Kia, supported by Ustun's disclosures, leads us to the conclusion that Petitioner's proffered rationale of data speed improvement is untenable on the present record.

Nevertheless, even if Ustun's data transfer speed were a reason to try a DMA-controlled FIFO configuration, Dr. Kia explains that Ustun's speed would not actually increase because the speed constraint in Ustun is

attributable to the Fast Fourier Transform calculations, which dictate the frame rate. *Id.* ¶ 95. In other words, speeding up the transfer of the initialization data would not change the speed at which the "real-time" images are obtained and displayed. We credit Dr. Kia's testimony on this issue over the testimony of Dr. Huber, which does not provide any details of the asserted implementation. *Compare* Huber Decl. ¶ 64 (stating in one conclusory sentence that a person of ordinary skill in the art would have known that DMA FIFO was particularly appropriate for transferring large amounts of data, such as the scanning data for OCT in Ustun) with Kia Decl. ¶¶ 94–95 (providing explanation of Ustun's operation and the alleged speed constraints in Ustun which would not be improved by implementing a DMA-controlled FIFO buffer). Thus, Patent Owner has shown persuasively the impact of Petitioner's reliance on a generic rationale of improving speed that is divorced from the realities of the application sought to improve. *See ActiveVideo Networks Inc. v. Verizon Comm., Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (finding that expert testimony of motivation to combine "to build something better," be "more efficient, cheaper, or" something that "had more features" was generic and insufficient). Accordingly, we are not persuaded that Petitioner's proffered rationale of improving data speeds is sufficient to implement a DMA-controlled FIFO buffer instead of the standard BlockRAM.

Third, Petitioner argues that implementing a DMA-controlled FIFO in Ustun would optimize the scanning data path, with a reasonable expectation of success. Pet. 17 (citing Huber Decl. ¶¶ 49–52). According to Dr. Huber, the asserted references address the same problem that the inventors of the '236 patent were trying to solve, "obtaining efficient and high performance electronics to generate, process, and output scanning OCT signals without

slowing down or interrupt a host processor." Huber Decl. ¶ 52. But as Patent Owner points out, a person of ordinary skill in the art would have recognized that Ustun does not attempt to solve the problem of a process interrupting the transfer of scanning data. PO Resp. 41. We agree with Patent Owner's assessment of Ustun.

Ustun is concerned with off-loading the FFT image processing from the host processor to the FPGA, which could work with a variety of external peripherals. Ustun at 2 (explaining that Ustun's approach is to rapidly process and display in real-time FDOCT images). By focusing on improving the processing path of image processing, *not the scanning data transfer*, Ustun's solution has nothing to do with optimizing the *output of OCT scanning signals* without slowing down the host processor, as asserted by Petitioner. Furthermore, Ustun's image processing is handled by the FDOCT peripheral, while the transfer of scanning data is processed via the Microblaze processor—thus, two separate processing entities are involved, neither of which would interrupt the other during the transfer of scanning data. *See* Ustun at 3 (explaining that the tasks of capturing images, executing the real-time FDOCT algorithm, and transferring the processed data to the computer are performed by the FDOCT peripheral in the FPGA fabric); *id.* at 4 (explaining that the coordination of low-speed data transfer for configuration and initialization from the host computer is handled by the Microblaze soft processor).

Additionally, as stated above, Ustun transfers the scanning data from the host processor once per scanning session, during initialization. *Id.* at 4 ("A serial communication scheme is sufficient in terms of speed because initialization parameters are transferred only once at the beginning of the data capture and processing cycle."). Thus, according to Dr. Kia's

testimony, which we credit, "Ustun's 'processing an image' will never interrupt the 'transferring of the scanning data' because these tasks are being performed by completely different processors." Kia Decl. ¶ 99; *see also id.* ¶ 100 (testifying that during the scan, the real-time processing of the images would not be affected by either calculations of scanning data or transfers of that data to the BlockRAM).

Accordingly, upon review of Petitioner's arguments summarized above and the arguments of Patent Owner in opposition, together with the evidence cited, we determine that Petitioner has not shown sufficiently, for purposes of institution, that a person of ordinary skill in the art would have had reason to implement in Ustun's BlockRAM a DMA-controlled FIFO. Neither a desire for higher speed data transfer, nor the need for optimization, proves to be a reason with rational underpinnings showing that a person of ordinary skill in the art would have understood Ustun to operate as Petitioner asserts. And asserting that DMA FIFO operation of a BlockRAM *could* have been implemented merely because it was known and doable does not show that a person of ordinary skill in the art *would* have done so. Consequently, we determine that Petitioner has failed to show a reasonable likelihood of prevailing on its assertion that Ustun and the asserted combination of teachings would have taught the "dedicated data buffer" recited in all challenged independent claims.

Culbertson is relied on for the teachings of stabilizing the eye position during an OCT scan as disclosing the use of the docking unit recited in claim 1. *See* Pet. 48–51. Petitioner does not rely on Culbertson as teaching the "dedicated data buffer." *See* Pet. 52 (addressing for claim 1 Ustun's teachings as described above). Therefore, our determination concerning the

deficiencies noted with respect to Ustun are not remedied by Petitioner's reliance on Culbertson.

Accordingly, we determine that Petitioner has not shown a reasonable likelihood of prevailing on its assertion that claims 1, 27, and 35 would have been unpatentable over Ustun, LabVIEW Help and Breyer. And for the same reasons, all the remaining grounds (all relying on Ustun as stated above) addressing the dependent claims also fail.

3. Additional Analysis for Claim 34

Claim 34 recites that the "output digital-analog converter is configured to output the scanning signals to x and y scanning controllers to scan an imaging beam; and synchronizing signals to an imaging camera to record a returned imaging beam synchronously with the scanning." Ex. 1001, 20:29–33. Petitioner relies on Hammer as teaching this limitation. In particular, Petitioner contends that Hammer outputs synchronization signals from the DAC to control the pair of galvanometers and the Cameralink[8] interface. Pet. 40 (citing Hammer at 5). We are not persuaded that Hammer supports Petitioner's contention.

Hammer, like Ustun, is an electronic board that processes OCT signals in real time for retinal tracking. Hammer at 5. Hammer states that the board has "2 DAC channels to control the OCT galvanometer pair and a Cameralink interface to collect raw spectral data from the linear detector and send processed depth scans to a framegrabber in a standard image acquisition (i.e., Cameralink) format." *Id.* This sentence does not state what Petitioner alleges—that the DAC output controls both the galvanometers and

[8] The Cameralink interface in Hammer and the Camera Link interface of Ustun appear to be the same thing despite their different spellings.

the Cameralink interface. The galvanometers, like in Ustun, are controlled by signals output through the DAC channels. But the Cameralink interface is controlled via the serial line, not the DAC channels. Hammer states for instance that "The Cameralink serial line is used both to control camera parameters . . . , but also to communicate image processing . . . and galvanometer control (e.g., scan type, amplitude, etc.) parameters between the host processor and the real-time board." *Id.* Thus, from these full disclosures, Hammer does not support Petitioner's assertion that the DAC outputs control signals for the Cameralink interface. Consequently, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that claim 34 would have been obvious as asserted.

4. Additional Analysis for Claim 18

Claim 18 recites that the "integration time of an image recording device is a limiting factor of an operating speed of an imaging system." Ex. 1001, 18:60–61. Petitioner relies on Ustun as disclosing this limitation. In particular, Petitioner points out Ustun's use of a FIFO memory buffer because the camera and the FPGA hardware work at different clock frequencies. Pet. 58. Dr. Huber testifies that Ustun's data processing clock speed of 100 MHz is limited by the maximum data transfer clock rate of the camera, 85 MHz. *Id.* Neither Petitioner nor Dr. Huber explain sufficiently how the data transfer clock rate of the camera is linked to the integration time of the camera. To the extent this explanation is part of the knowledge that a person of ordinary skill in the art would have, it is incumbent upon Petitioner to explain that knowledge in the Petition. Indeed, the lack of explanation in the Petition is even more evident in light of Ustun's disclosure that the integration time is one of the base parameters that the

initialization program converts from user selected parameters. Ustun at 6. Without any explanation, the record before us lacks evidence showing that Ustun's integration time is a limiting factor as the claim requires. Consequently, we determine that Petitioner has failed to show a reasonable likelihood of prevailing on its assertion that claim 18 would have been obvious as asserted.

5. Conclusion

Upon review of the Petition, and the information presented in the Preliminary Response, we determine that the Petition fails to meet the reasonable likelihood threshold of institution.[9] As stated above, we find that the Petition lacks evidence that Ustun teaches a FIFO buffer, or any other buffer for that matter, that holds and outputs scanning data, or that it would have been obvious to implement a DMA controlled FIFO buffer as asserted because the Petition does not present a reasonable rationale, with rational underpinnings, supporting the combination of teachings. We also determine that the Petition fails to show how the limitations further recited in claims 34 and 18 are taught by the prior art.

IV. CONCLUSION

As stated in the paragraph above, we conclude that Petitioner has not demonstrated a reasonable likelihood of prevailing on its assertion that the challenged claims are unpatentable as asserted. Accordingly, we deny the Petition.

[9] Patent Owner presents additional arguments concerning discretionary denial under 35 U.S.C. § 325(d). Because we determine that the Petition is deficient on the merits, we need not address that issue.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is denied.

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